

Compal Confidential

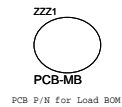
QCL90 MB Schematic Document

LA-8223P

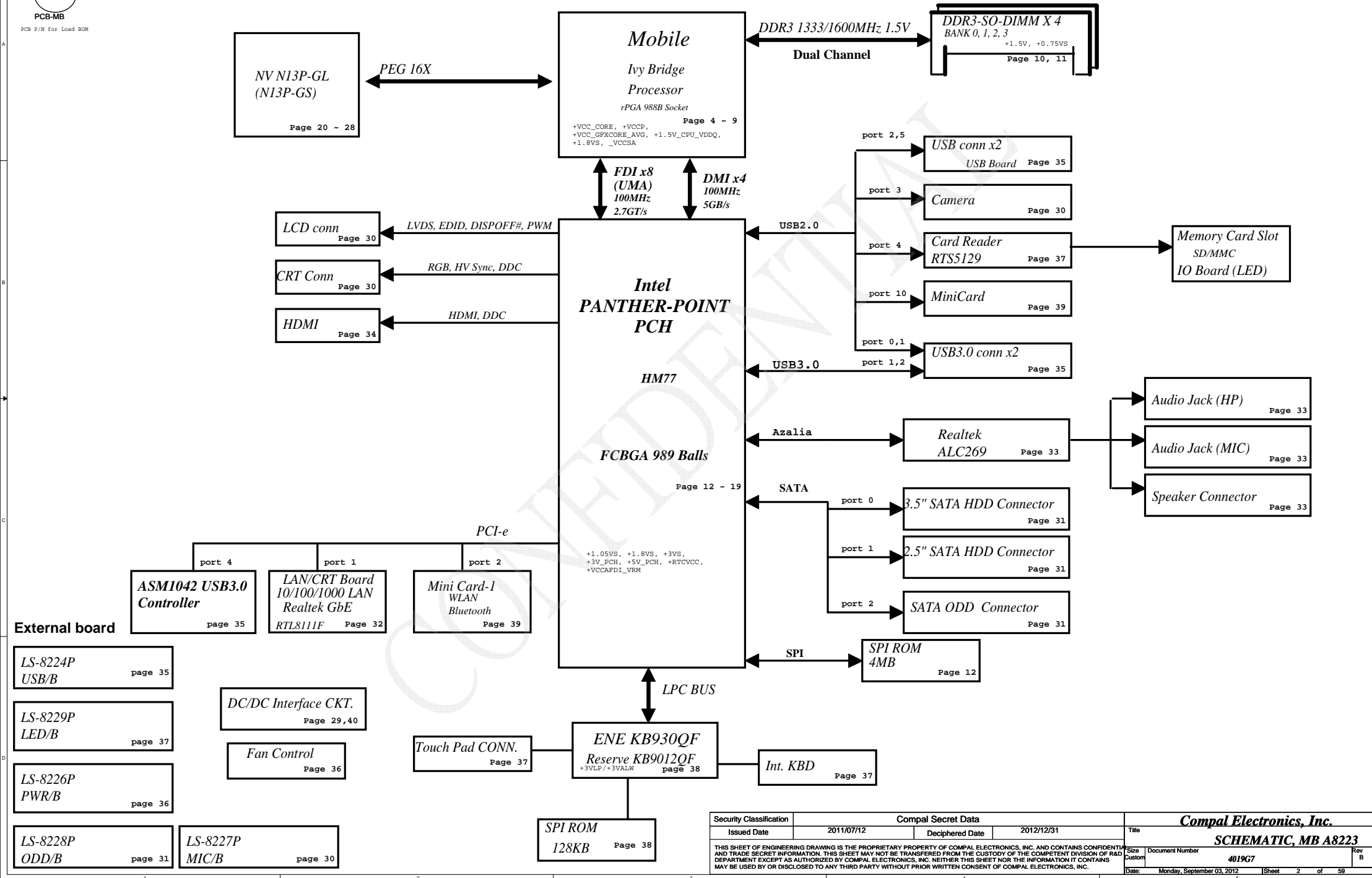
Rev: 1.0

2012.01.19

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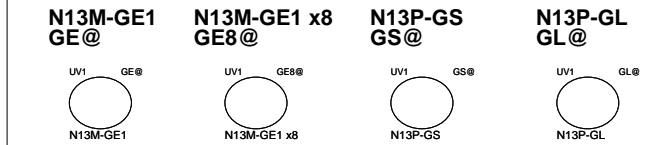
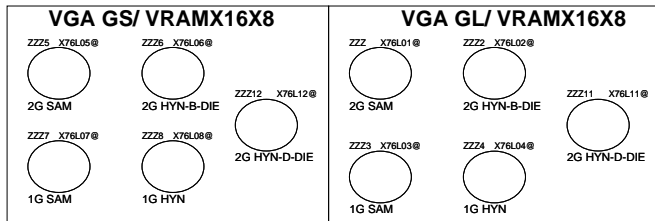


QCL90



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X76@:

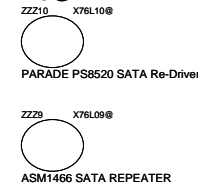


GEL@: N13M-GE1 or N13P-GL
GS@: N13P-GS
DIS@: VGA componet
9012@: EC(ENE 9012 chip)
930@: EC(FNF 930 chip)

USB30@: USB3.0 by ASMEDIA
IU3@: USB3.0 by PCH

AI@: AI Charger
NAI@: Non AI Charger

SATA Re-Driver X76@





SMBUS Control Table

	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	X	X	V
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	X	X	V	X
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	V	X	V

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	ASMEDIA USB3.0	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

 : means Digital Ground

 : means Analog Ground

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

Voltage Rails

Power Plane	Description	S1	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 510N power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	ON	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for DDR SPI,PCH,HDD,Audio,Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VGA	ON	OFF	OFF	OFF
+LCDVDD	3.3V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD,AUDIO,FAN,Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU,PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO,PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH,WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORE_AXG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics ON OFF OFF	ON	OFF	OFF	OFF

SATA	DESTINATION
SATA0	3.5" HDD
SATA1	2.5" HDD
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCH	USB3 PORT	DESTINATION
	1	USB2.0+3.0
	2	USB2.0+3.0
	3	None
	4	None

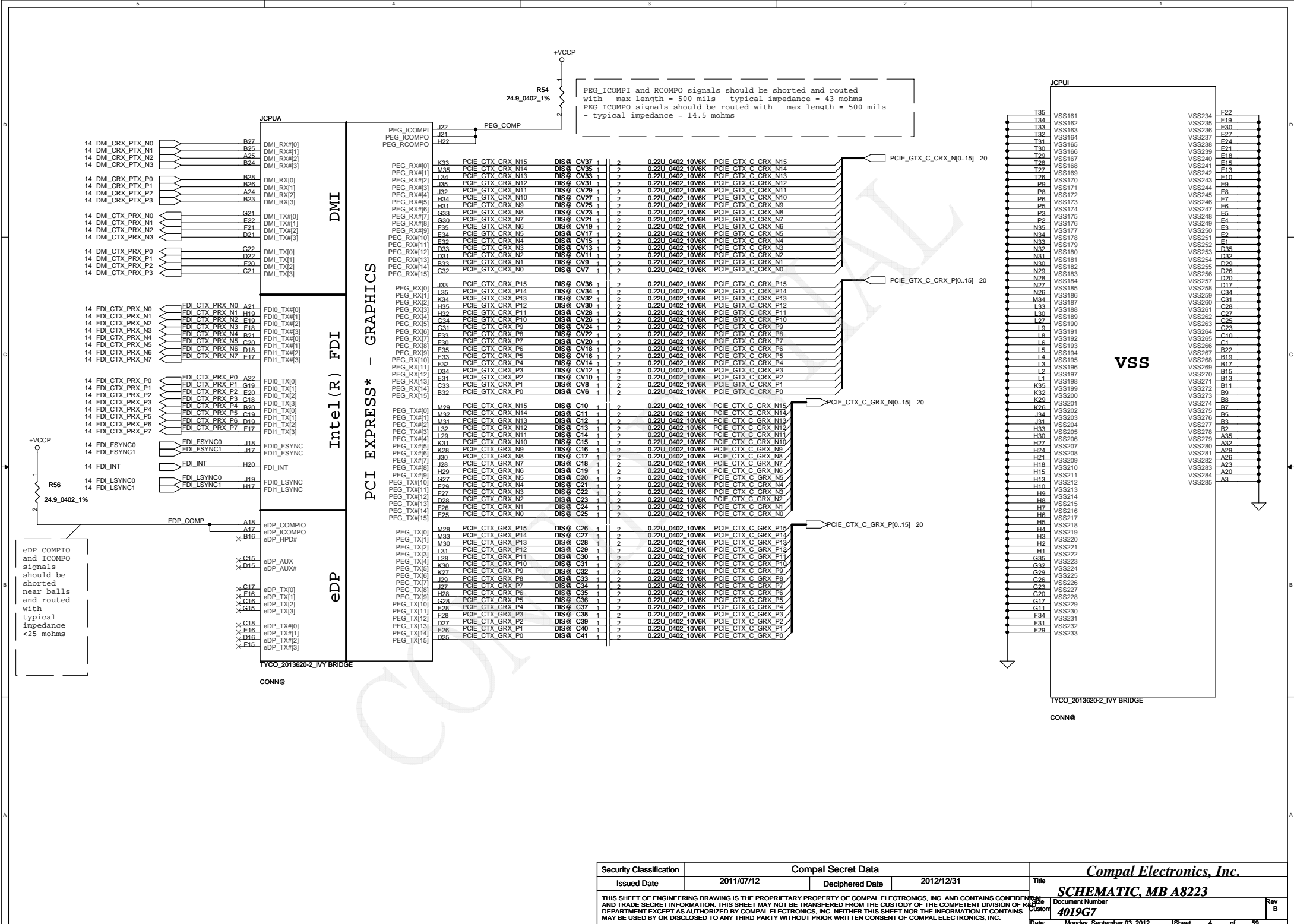
PCH

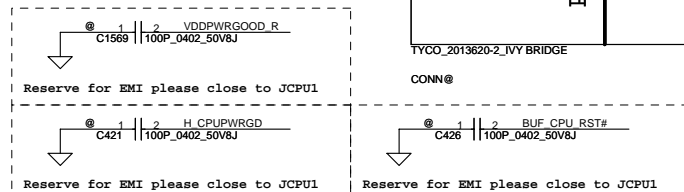
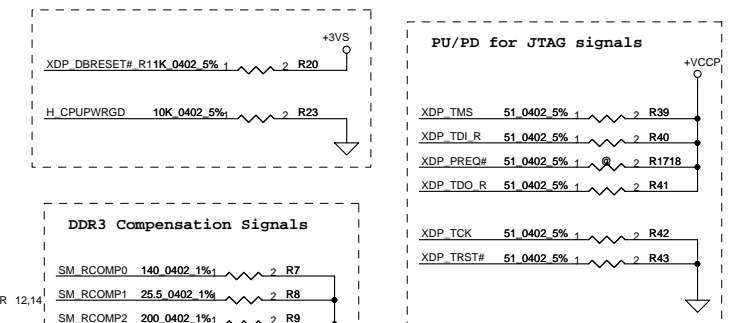
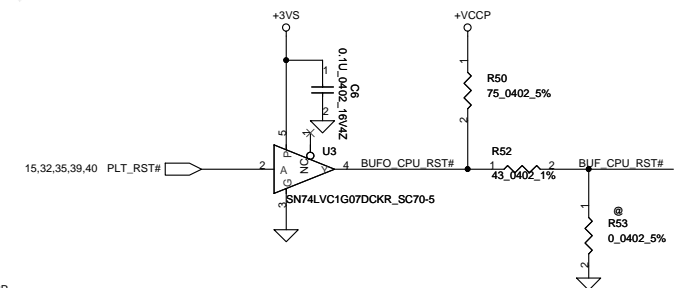
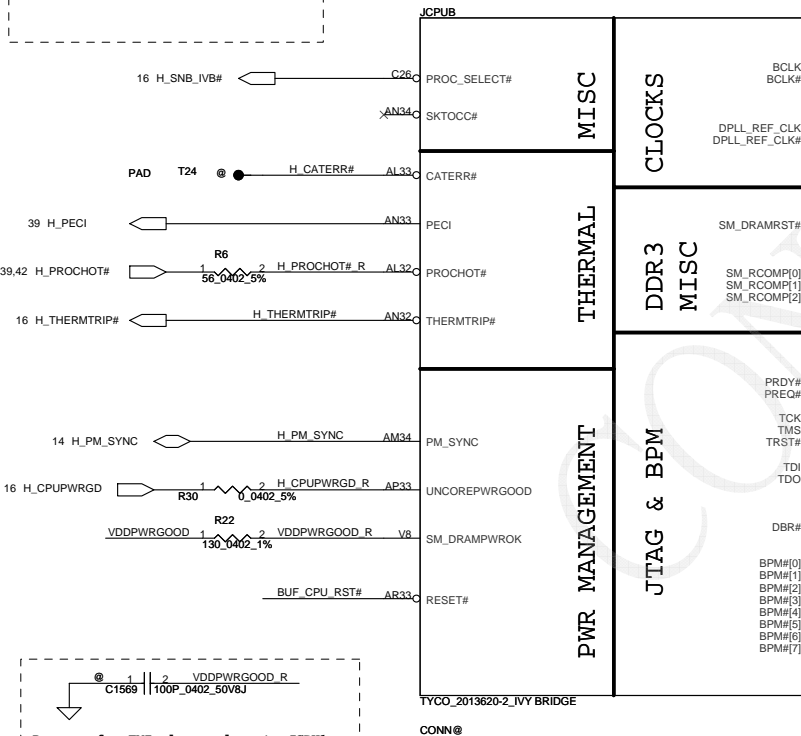
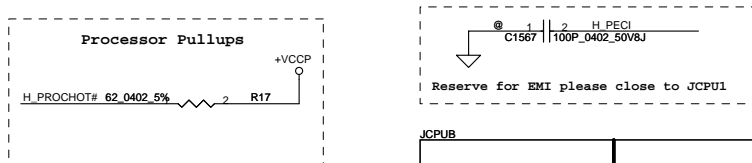
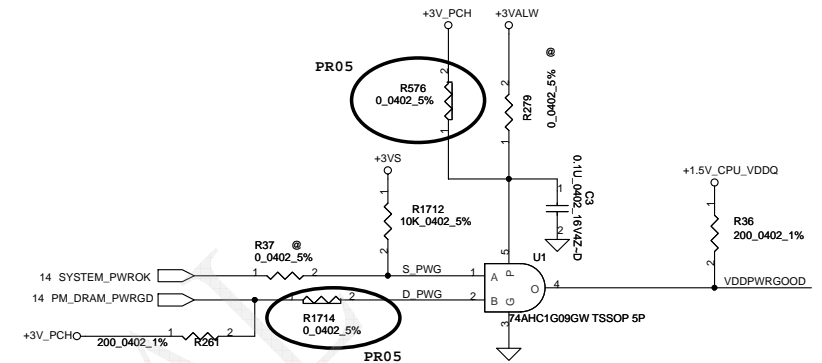
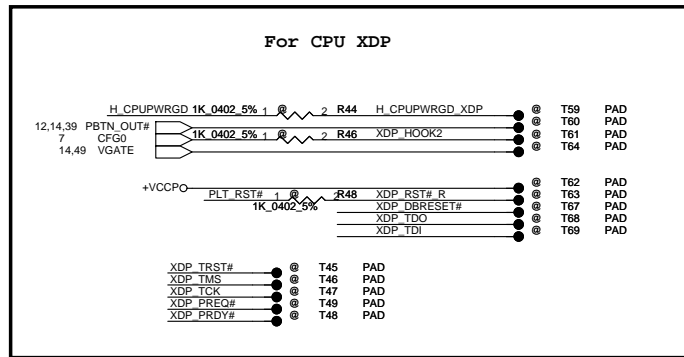
PCH	USB2 PORT	DESTINATION
	0	USB2.0+3.0
	1	USB2.0+3.0
	2	USB2
	3	CAMERA
	4	Card Reader
	5	USB2
	6	None
	7	None
	8	None
	9	None
	10	JMINI1 (WLAN) Bluetooth
	11	None
	12	None
	13	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD WLAN
Lane 3	None
Lane 4	ASMEDIA USB3.0
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

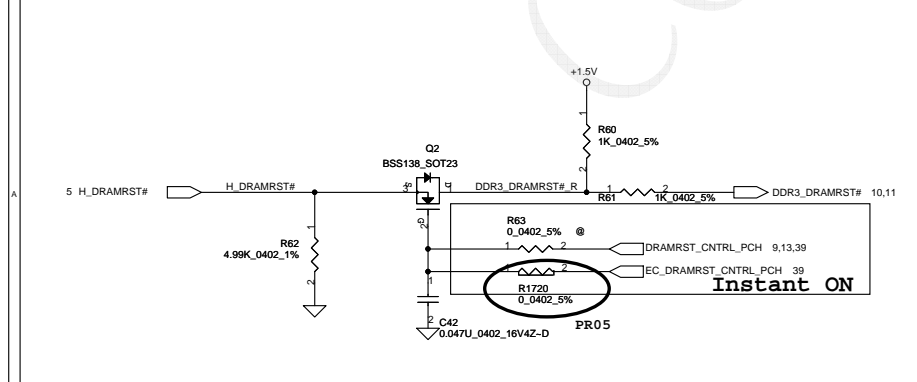
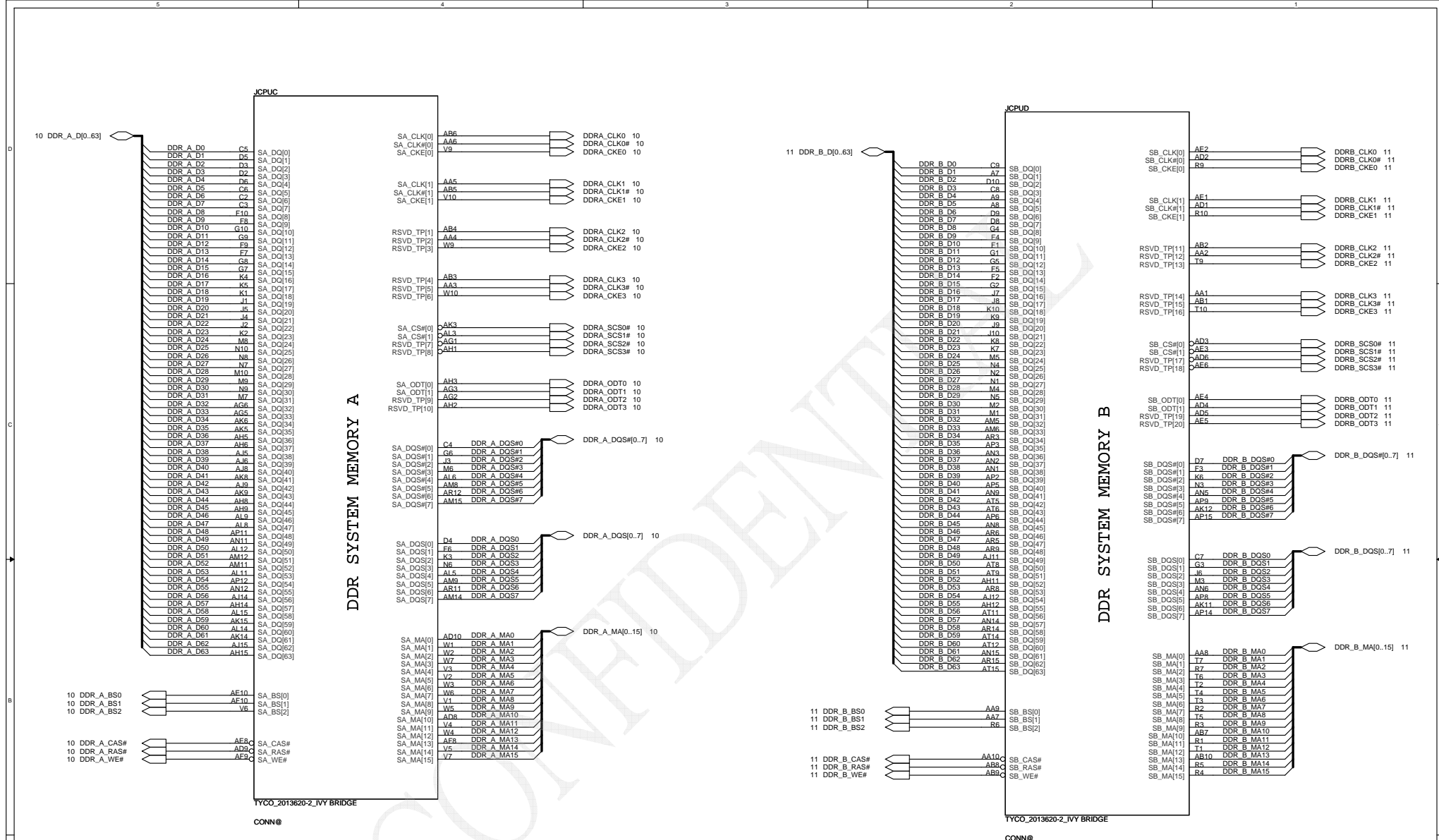
QCL90 * 16 (LA8223P) Board ID Table for AD channel

Vcc	3.3V +/- 5%	typ: 0.958~1.359V		
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
*	56K +/- 5%	0.958 V	1.185 V	1.359 V



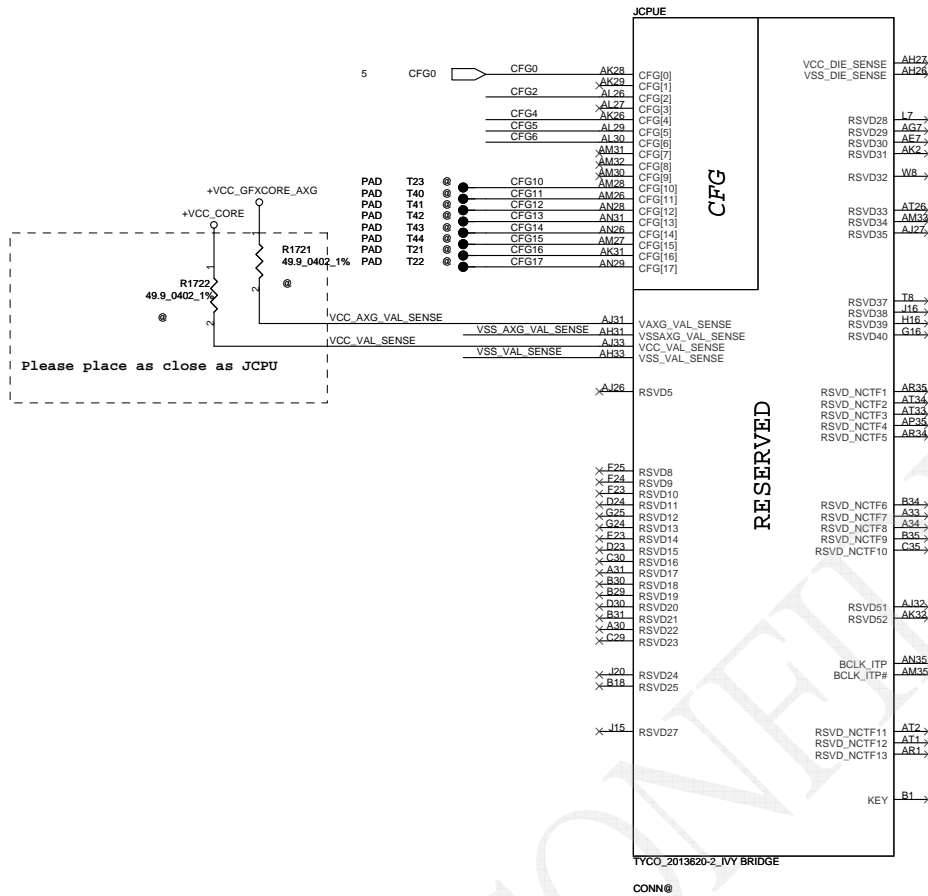


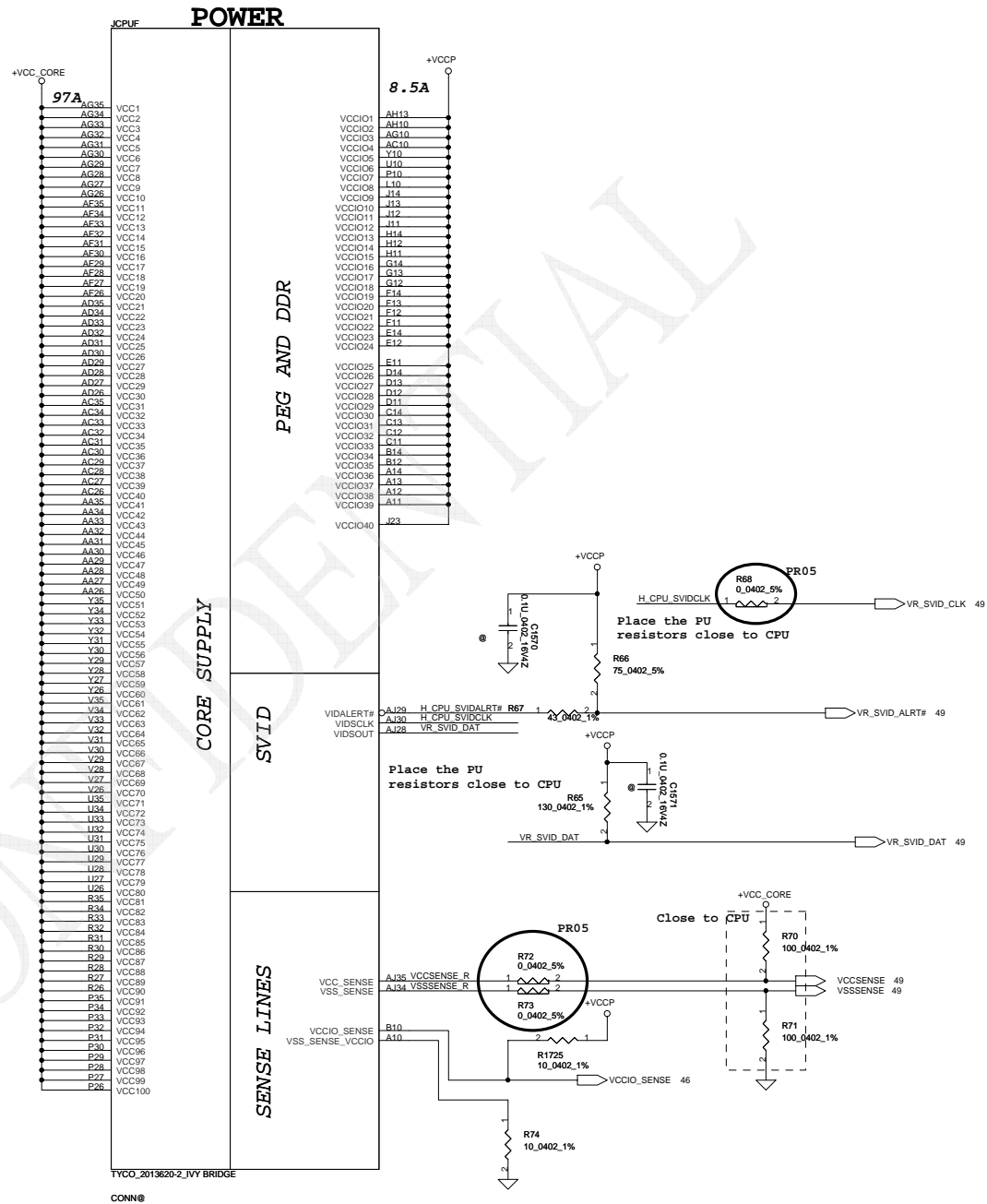
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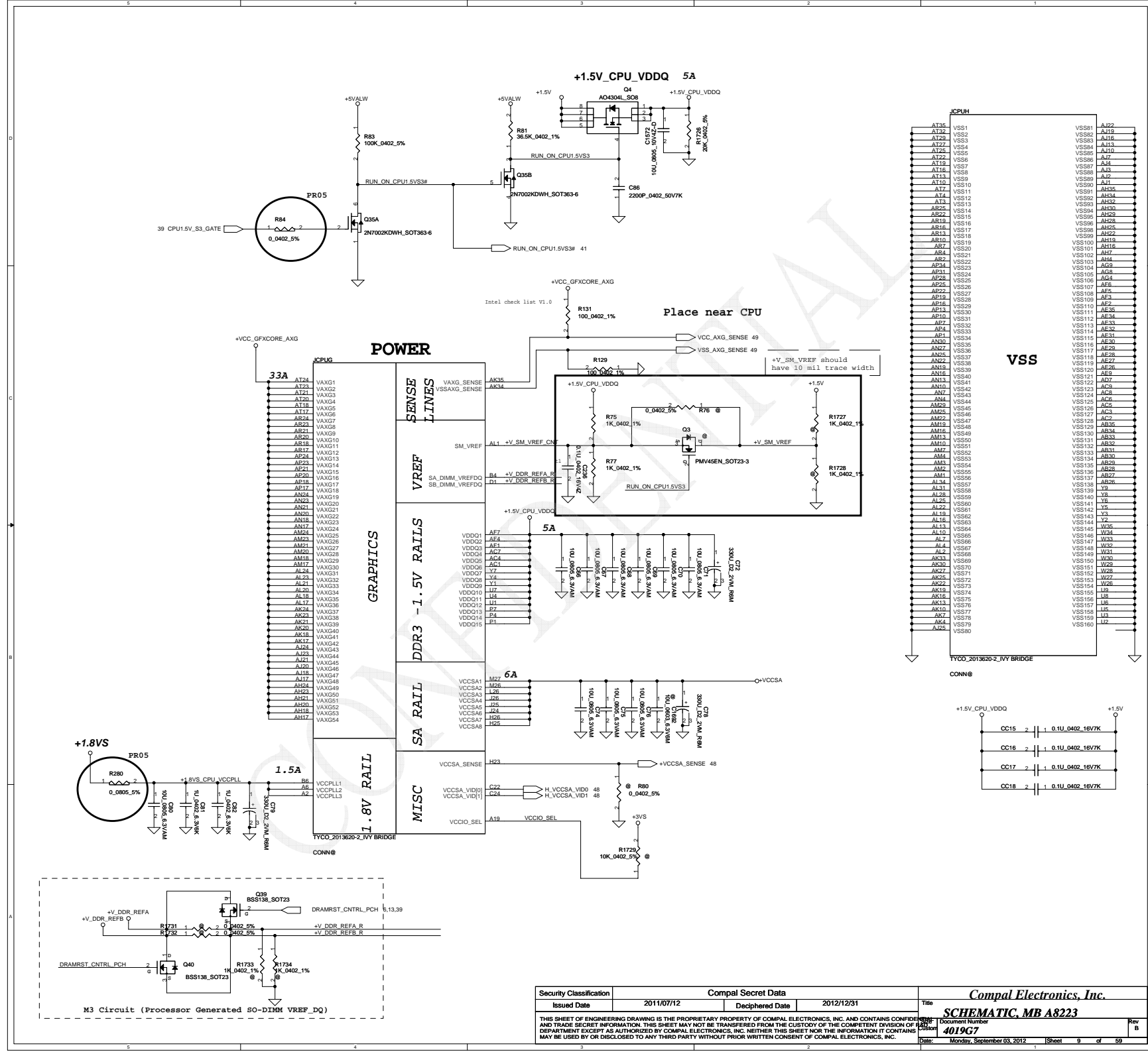
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CFG Straps for Processor



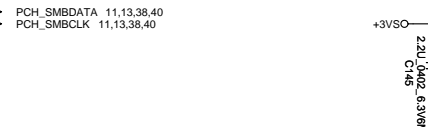
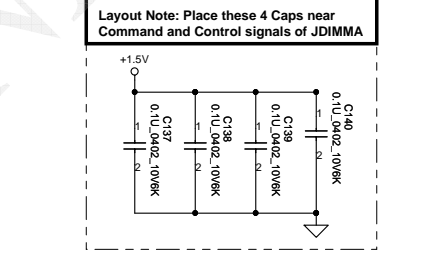
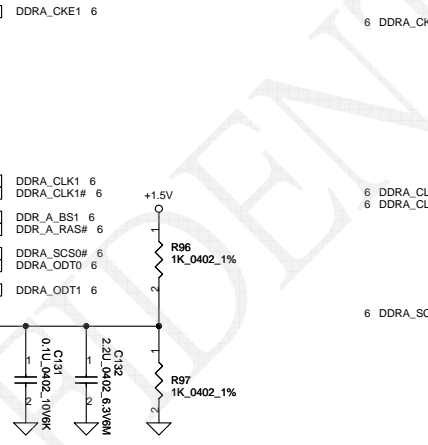
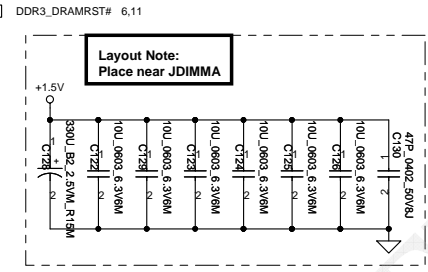


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Support SO DIMM X 4 Support 1066/1333MHz

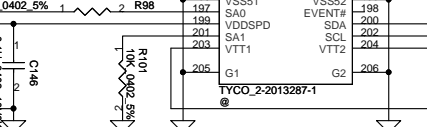
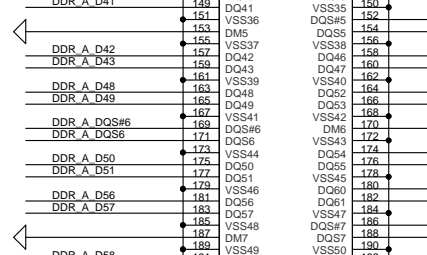
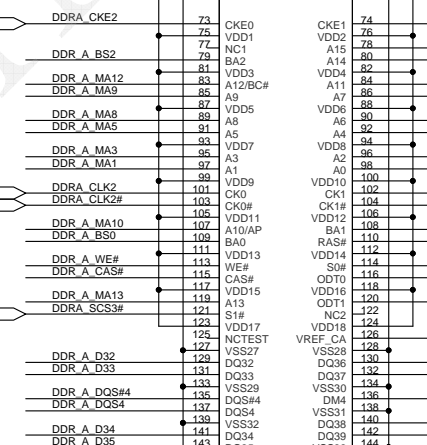
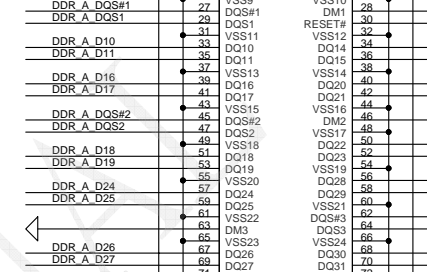
6 DDR_A_D[0..63]
6 DDR_A_DQ[0..7]
6 DDR_A_DQS[0..7]
6 DDR_A_DQS#0..7
6 DDR_A_MA[0..15]



Standard: 5.2mm
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BOT

Support SO DIMM X 4 Support 1066/1333MHz

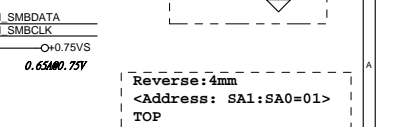
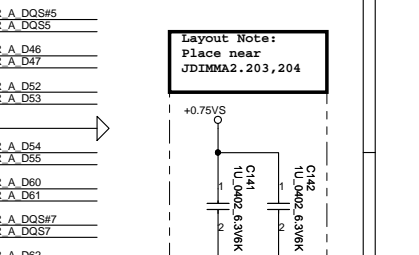
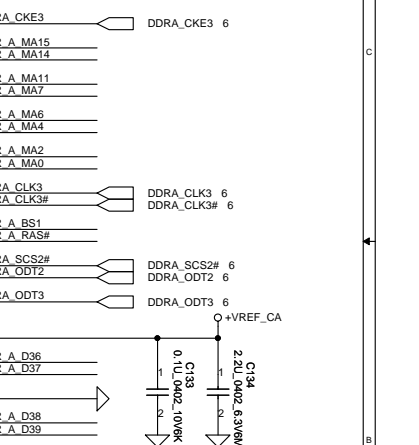
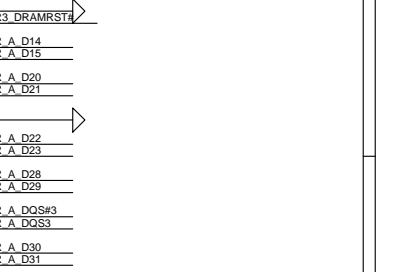
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6 DDR_A_DQS#0..7
6 DDR_A_MA[0..15]



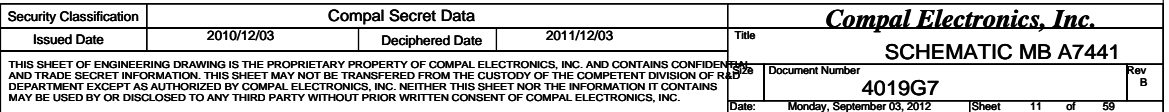
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Support SO DIMM X 4 Support 1066/1333MHz

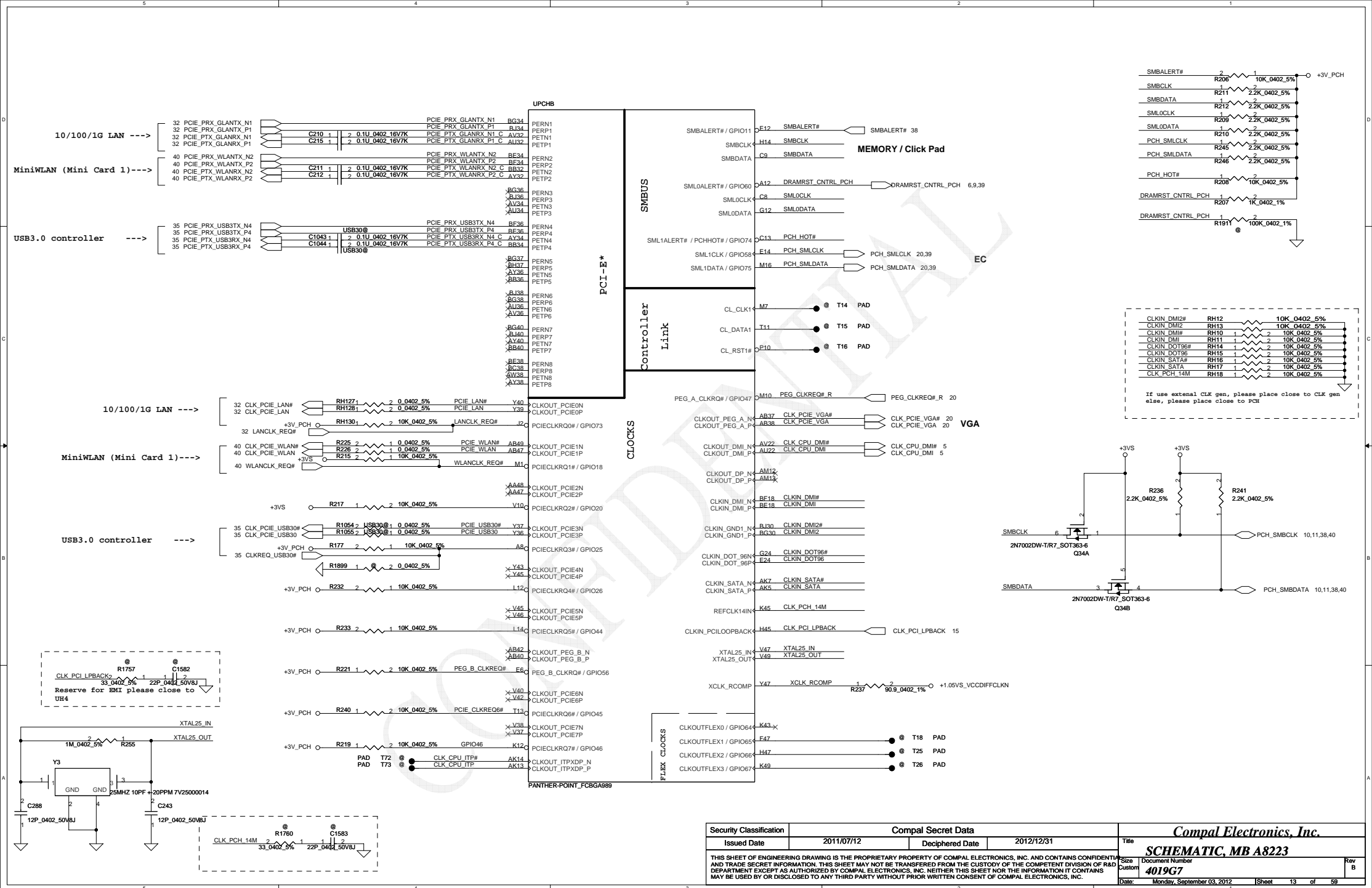
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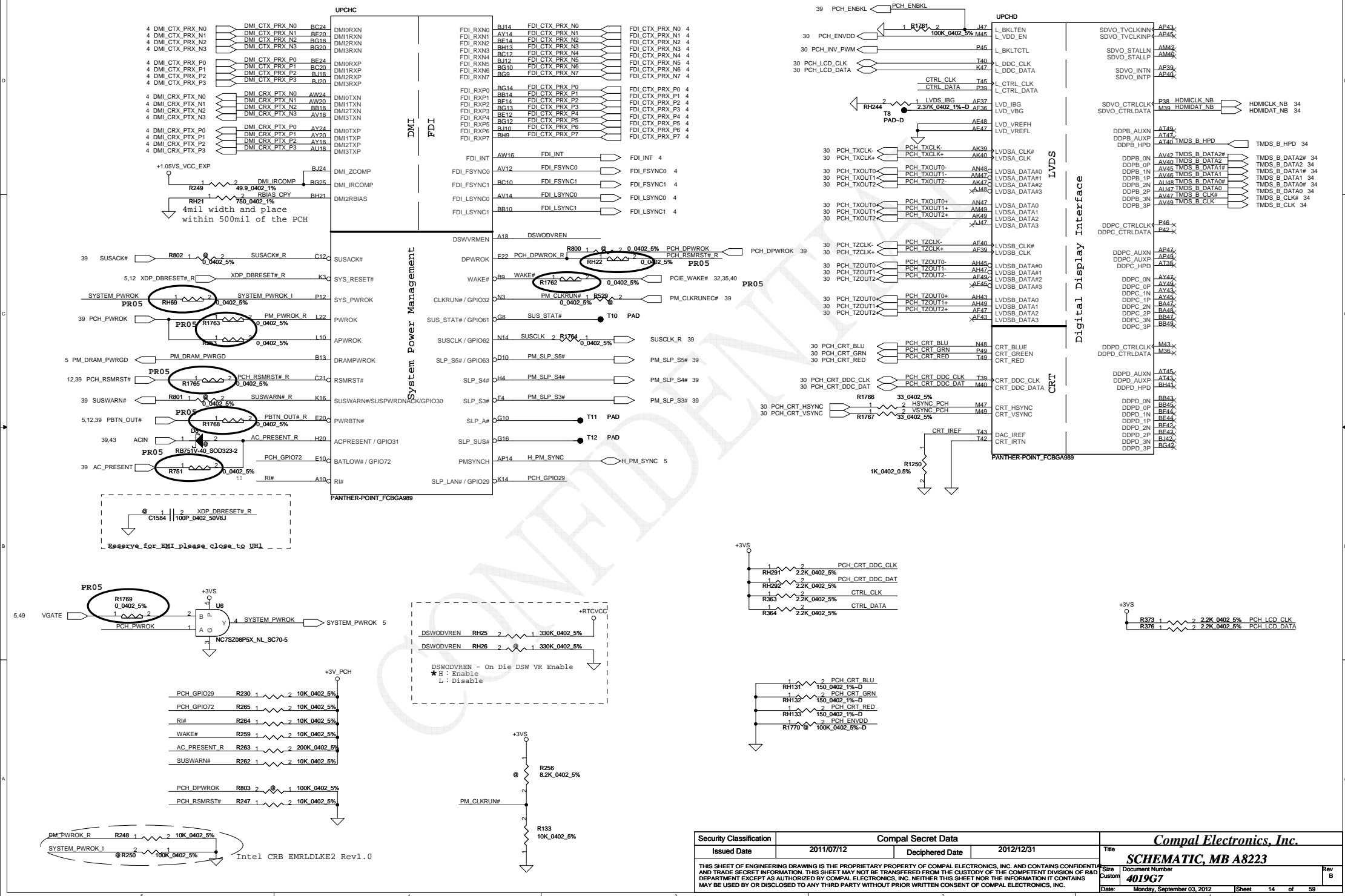
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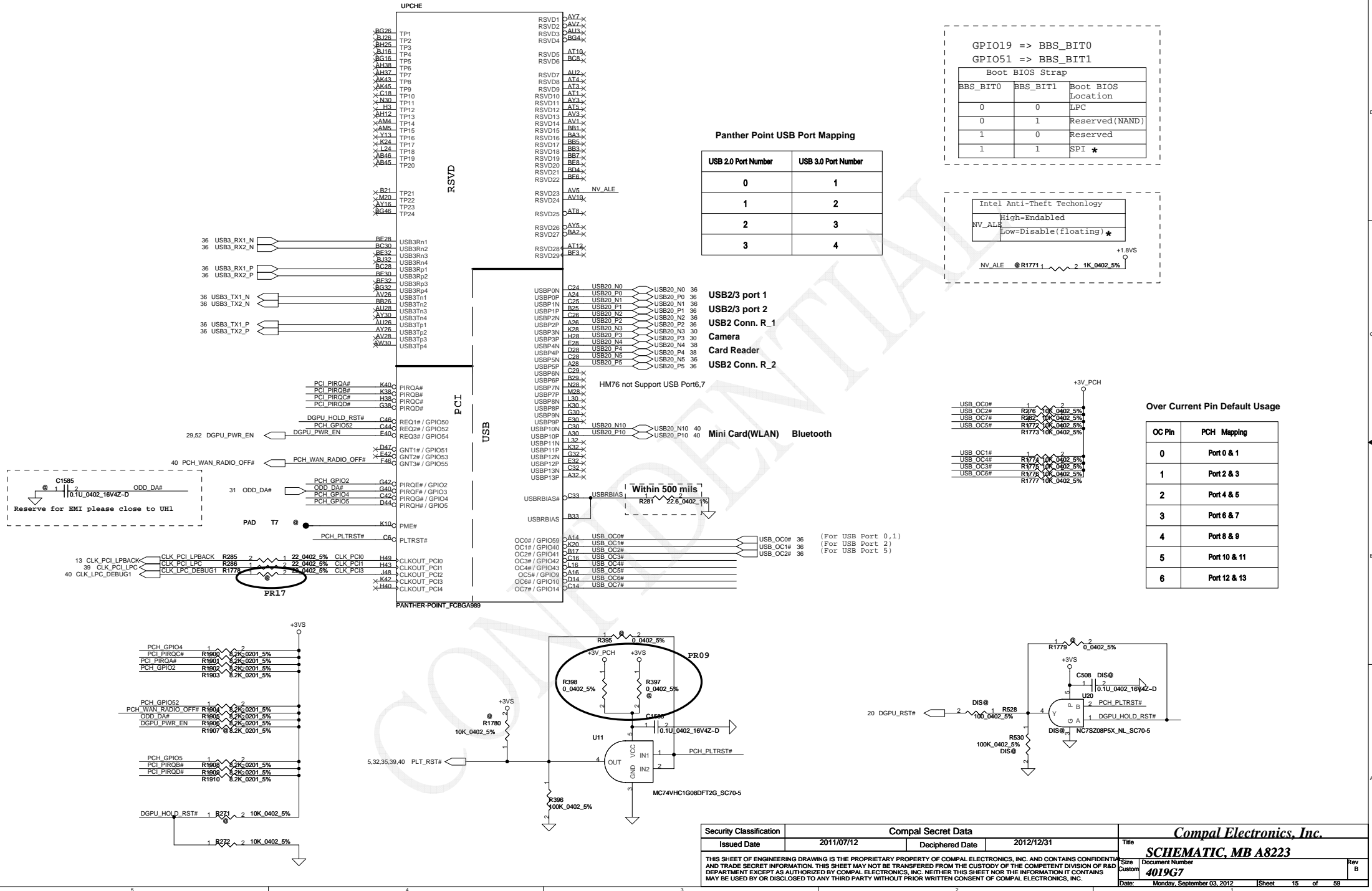


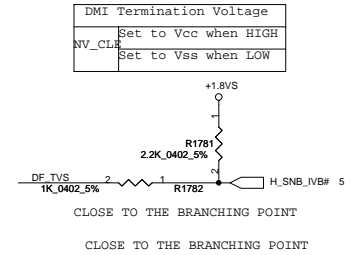
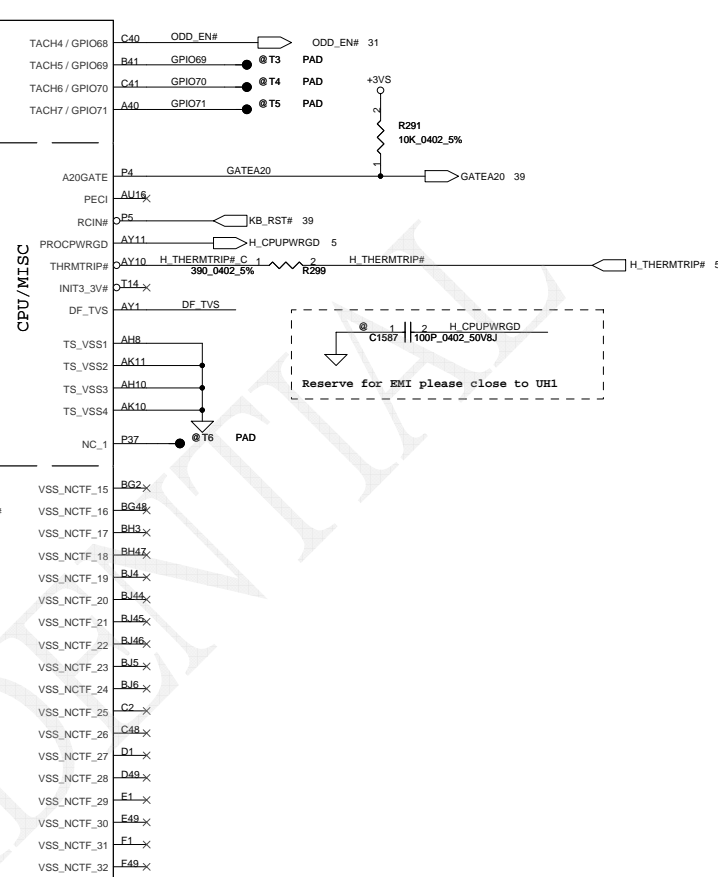
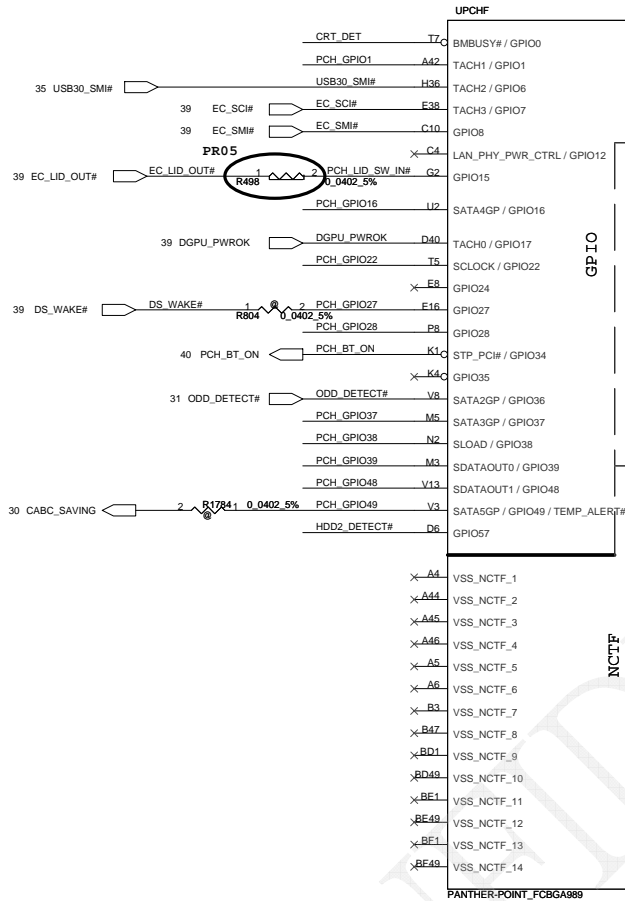
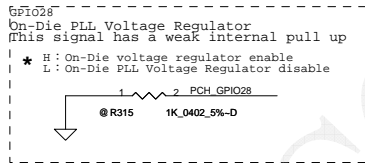
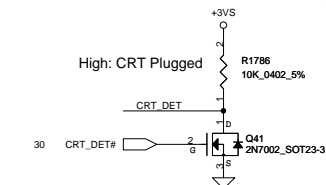
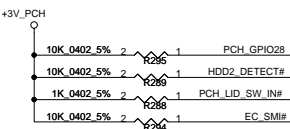
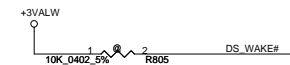
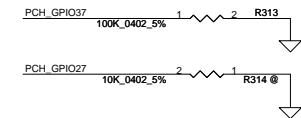
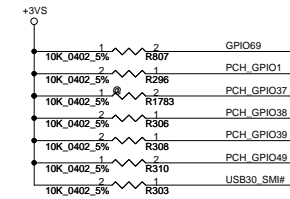
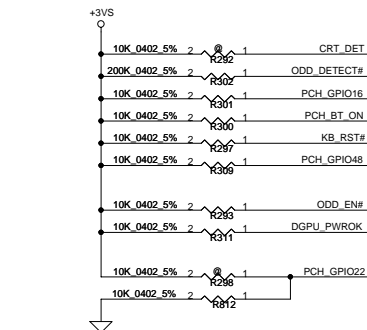
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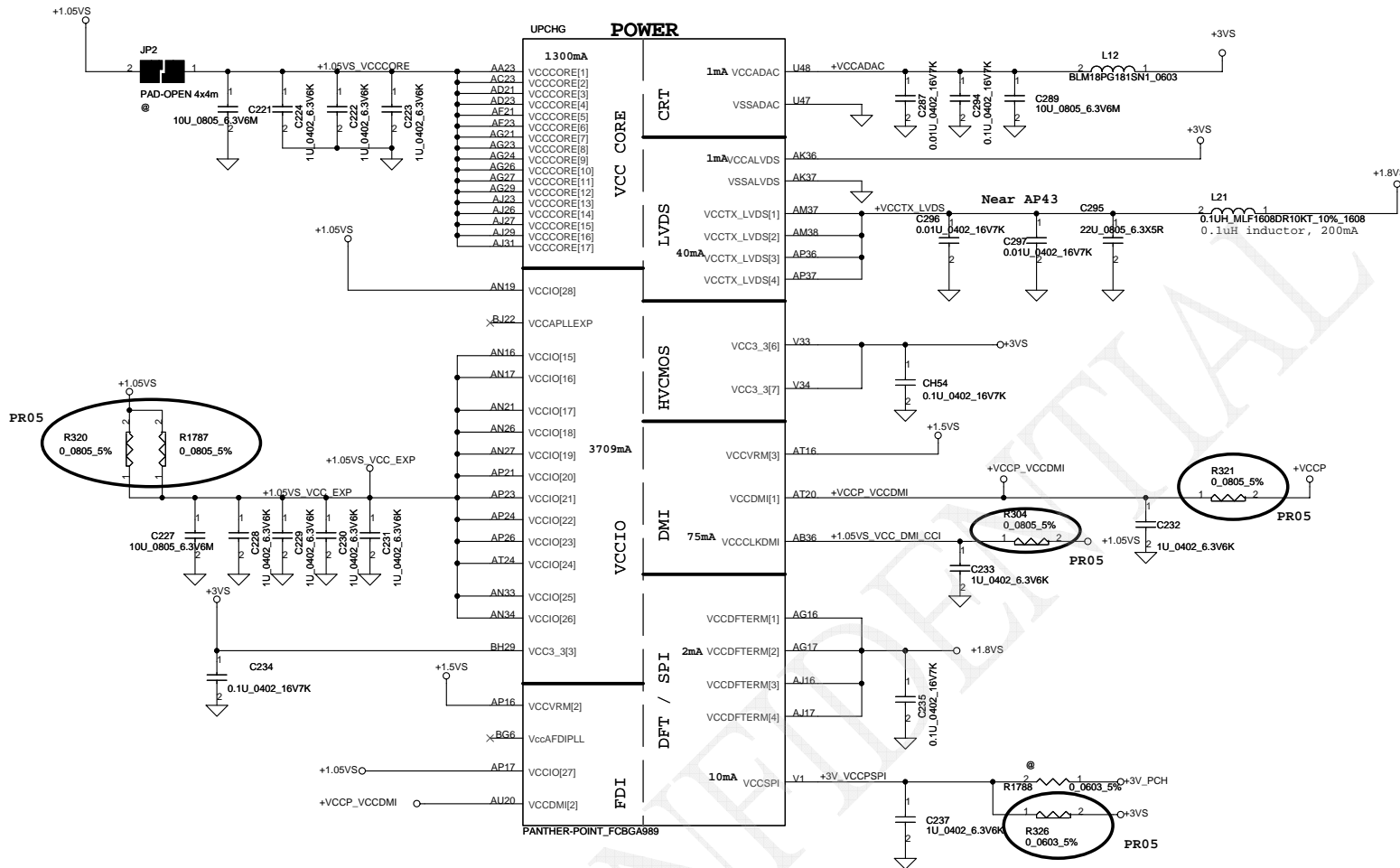
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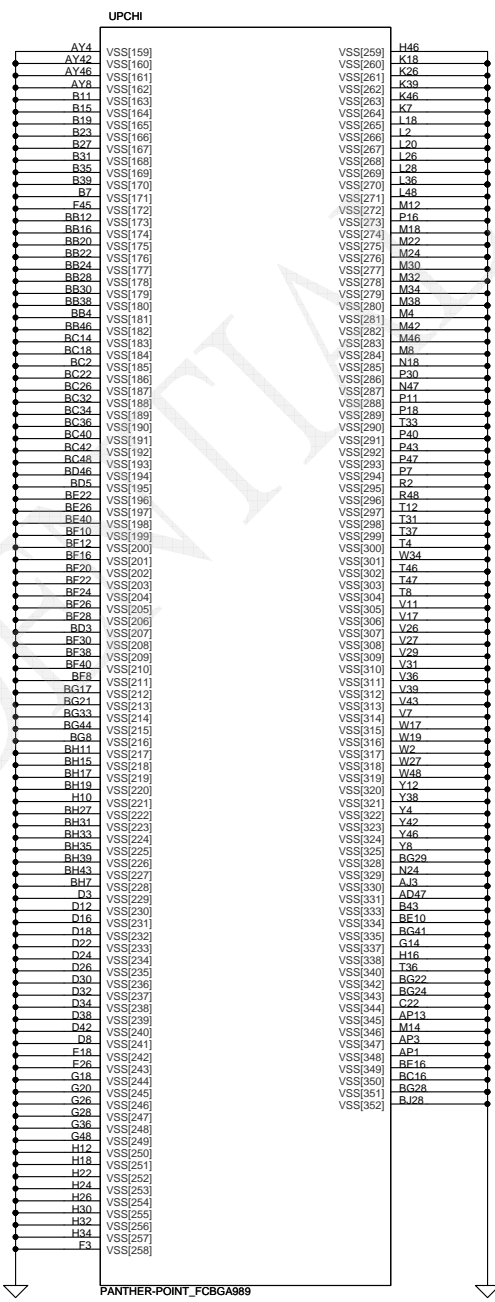
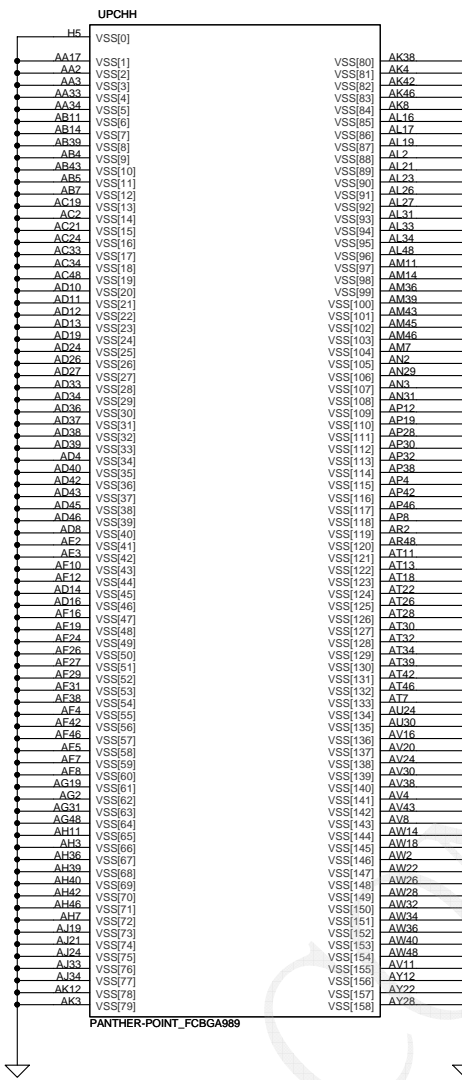


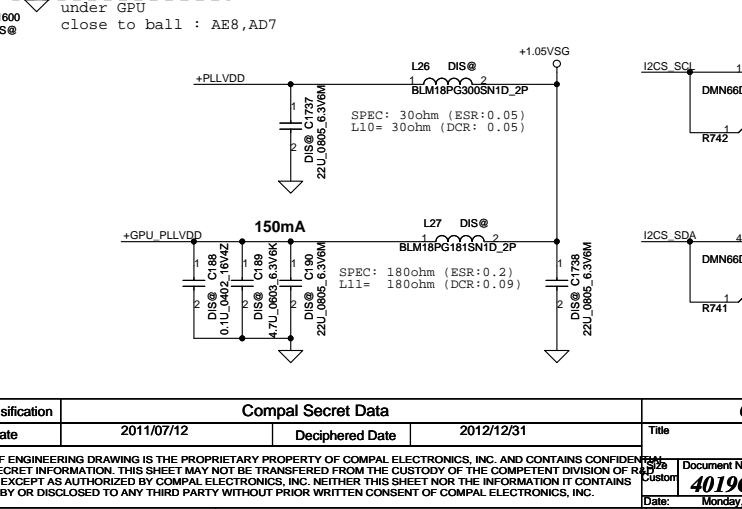
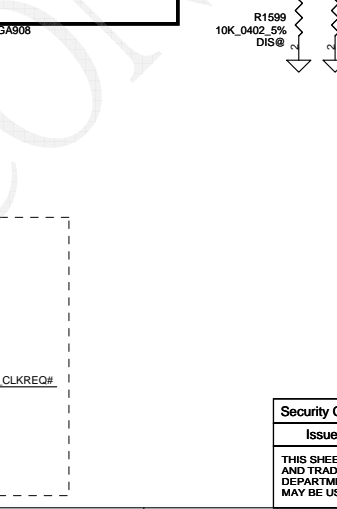
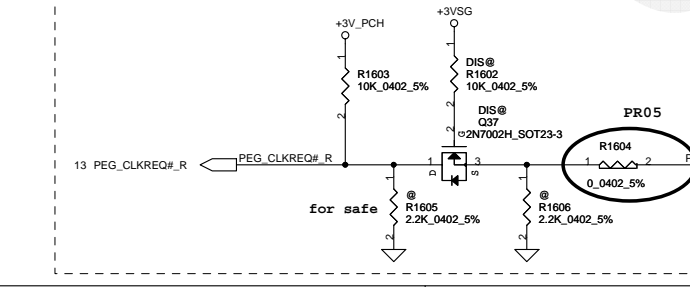


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PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTerm	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04





SG
)

6

W-7_SOT363-6
2A GEL @

2
@ 0_0402_5%

PCH_SMLCLK 13,39

SG
)

3

W-7_SOT363-6
2B GEL @

2
@ 0_0402_5%

PCH_SMLDATA 13,39

mpal Electronics, Inc.

SCHEMATIC, MB A8223

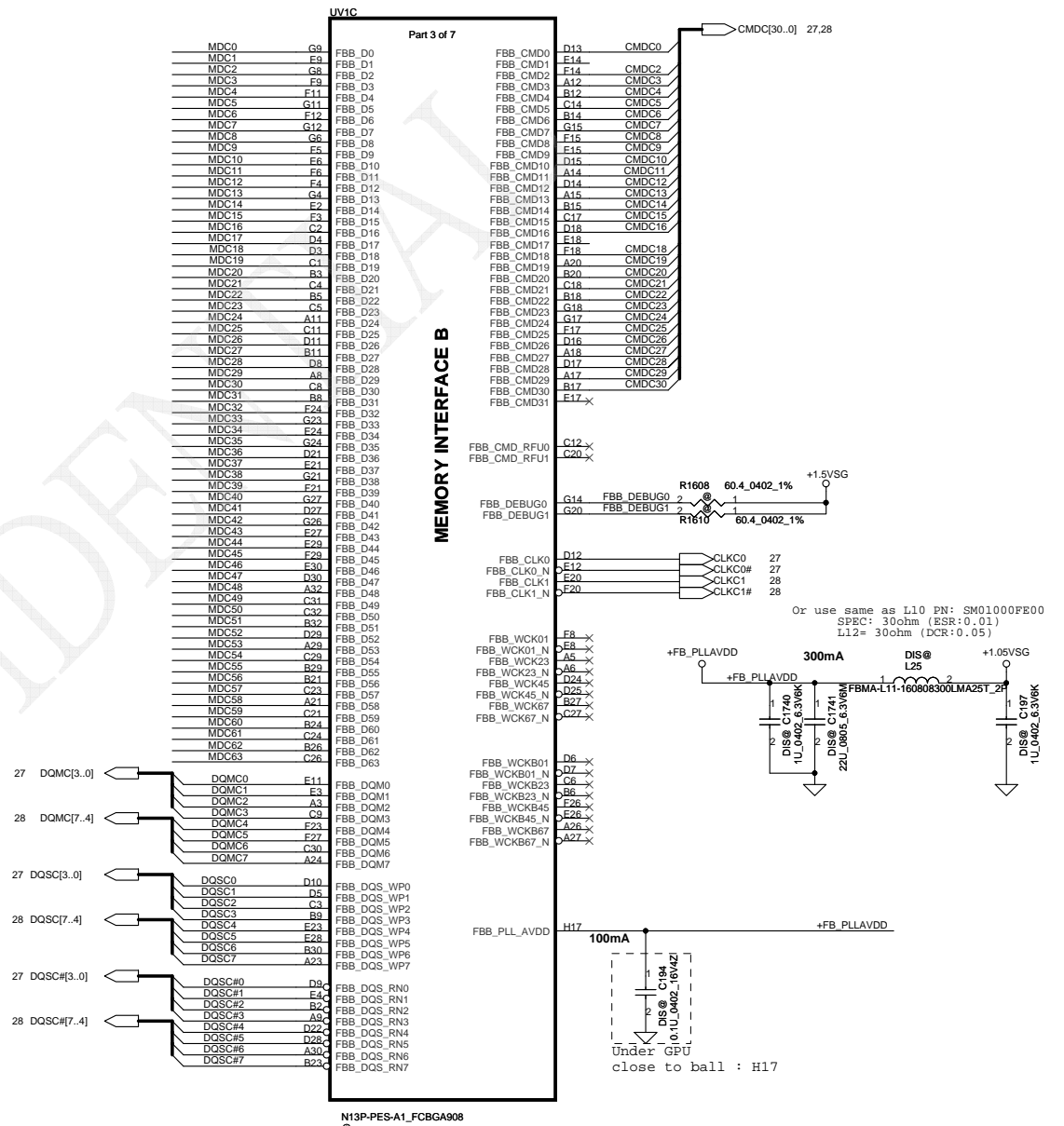
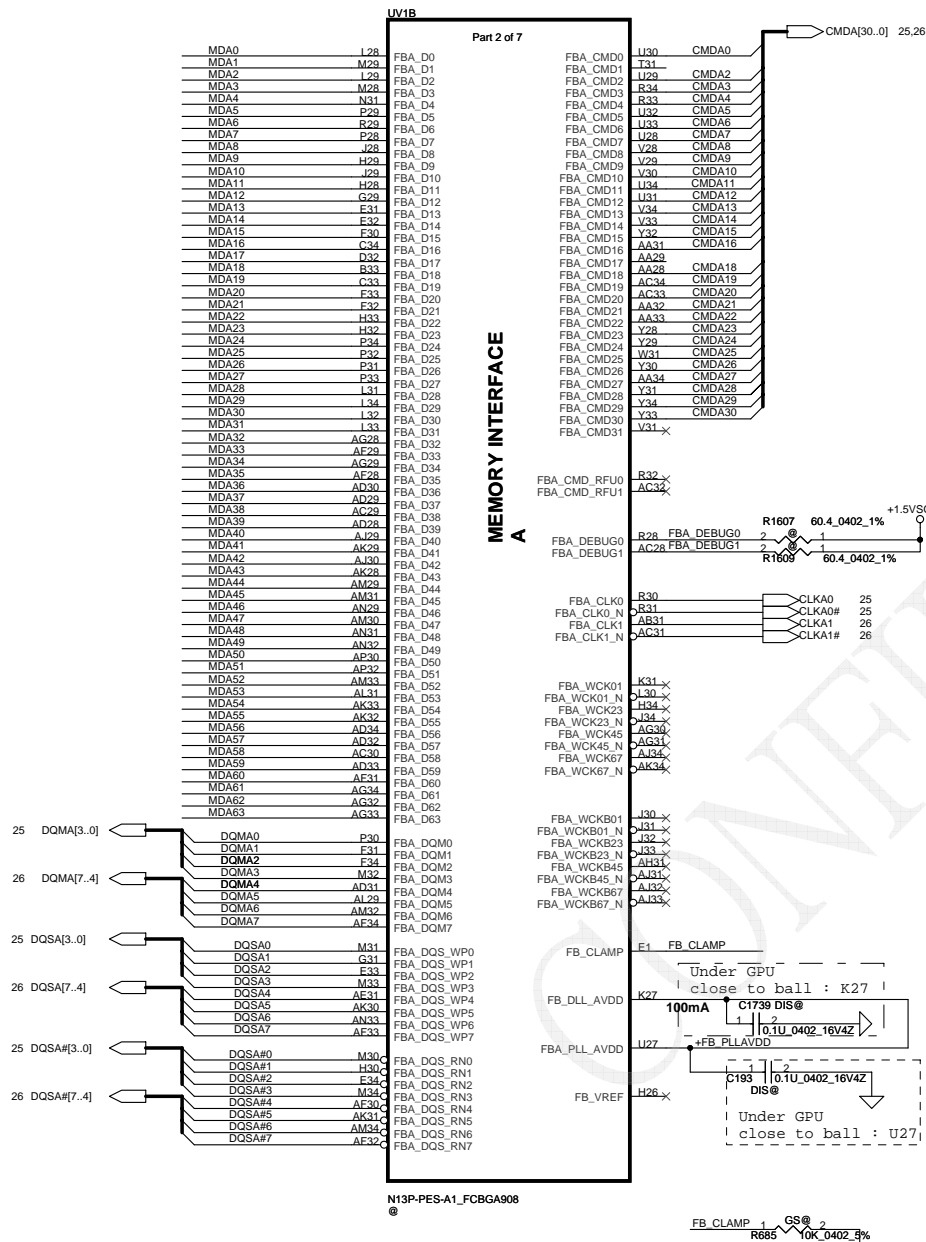
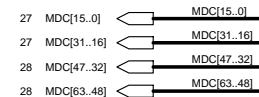
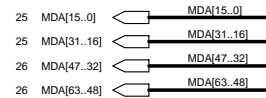
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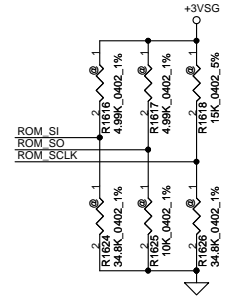
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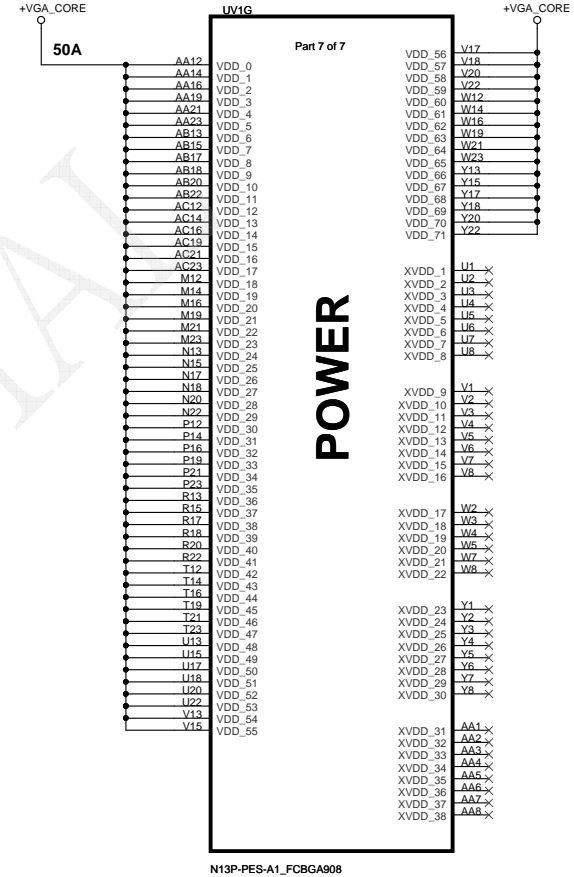
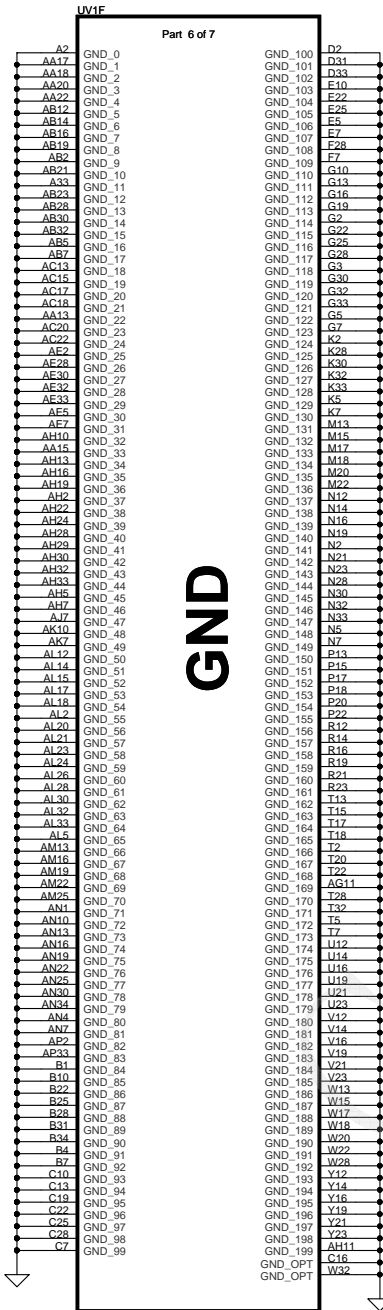
VRAM Interface



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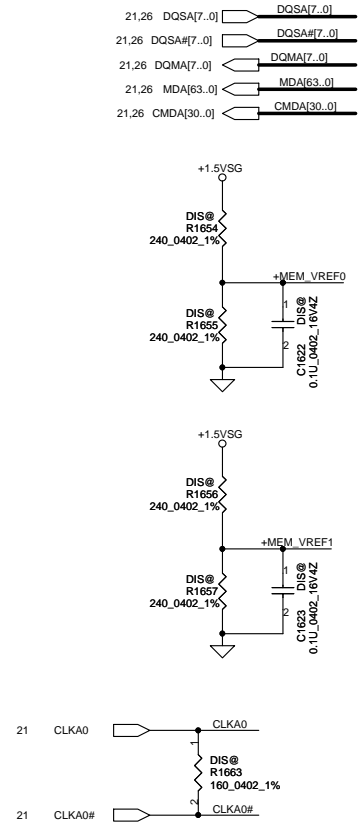
GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE1	900 MHz	256M* 8" 8 2GB	ELPIDA SA000056700	R PU 45K	R PD 35K	R PU 5K	R PD 5K	R PD 10K	R PD 5K	R PU 10K	R PU 5K
N13M-GE1	900 MHz	256M* 8" 8	Synacore	R PU 145K	R PD 35K	R PU 5K	R PD 5K	R PD 10K	R PD 10K	R PU 110K	R PU 5K



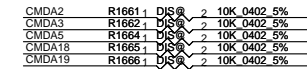
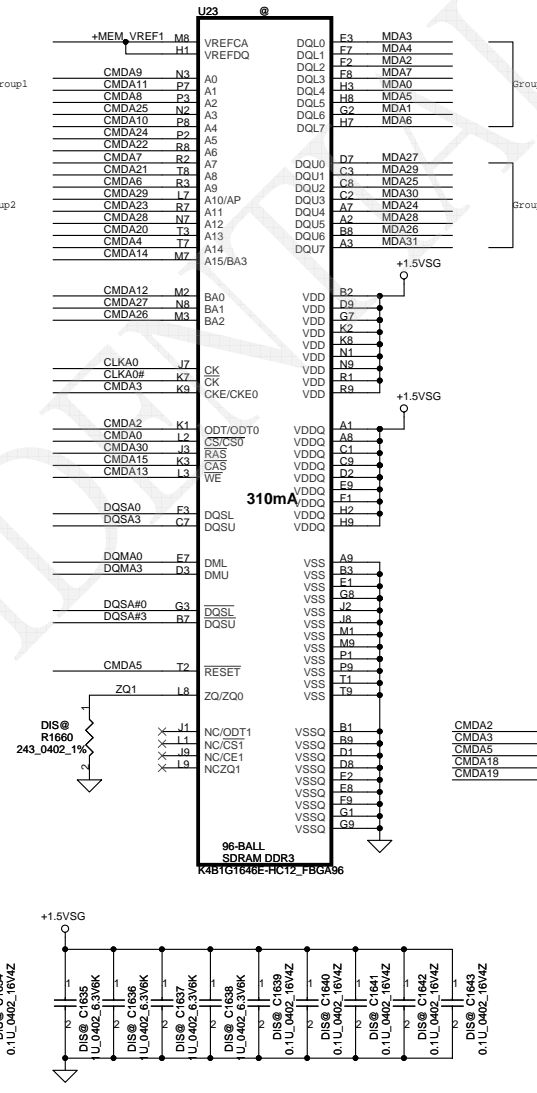
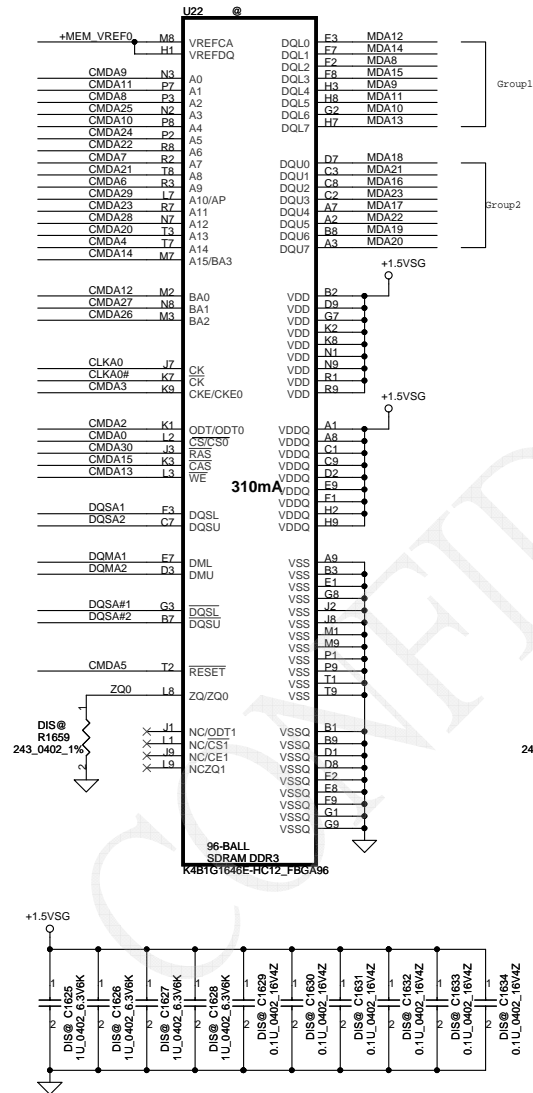
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VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB



NV recommend 0720



Command Bit	Default Pull-down
ODT#	10k
CKE#	10k
RST	10k
CS*	No Termination

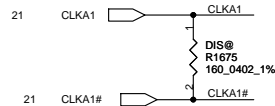
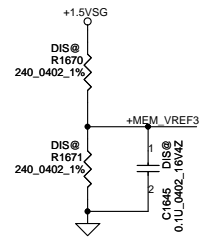
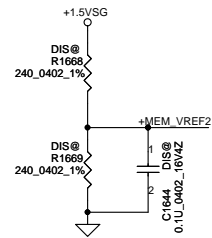
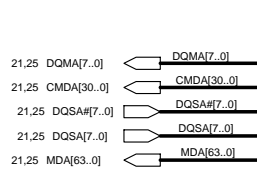
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1648E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFPGA 96P 1.5V)

Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

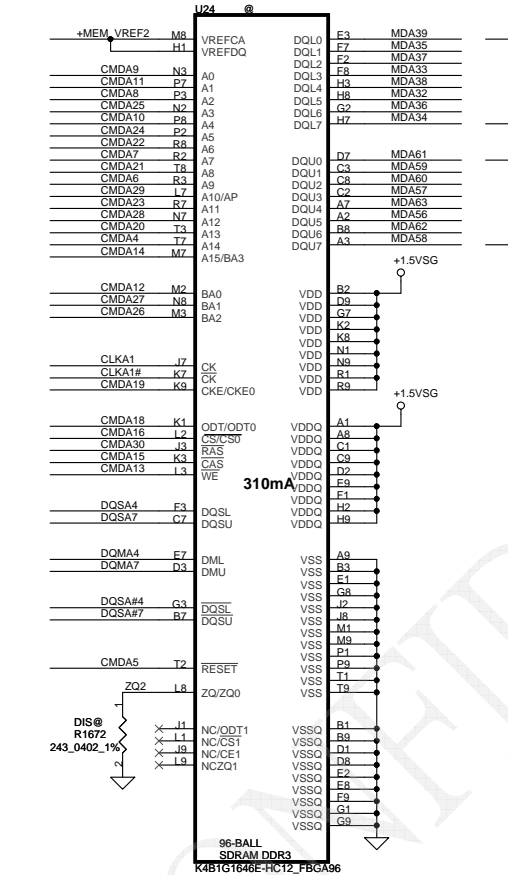
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

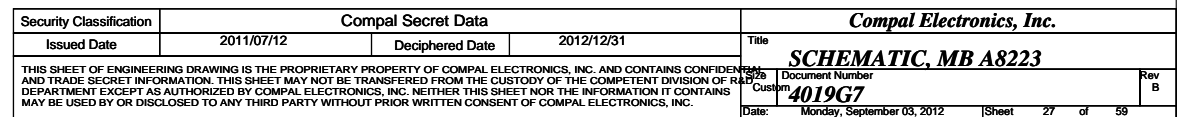
128Mx16 DDR3 *8==>2GB



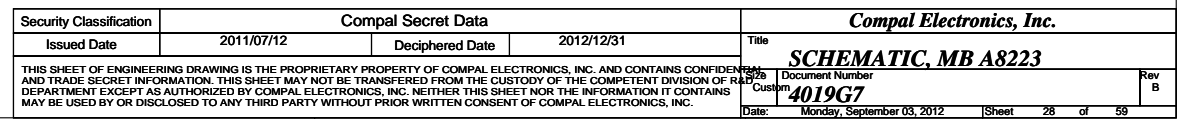
WV recommend 0720



64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB



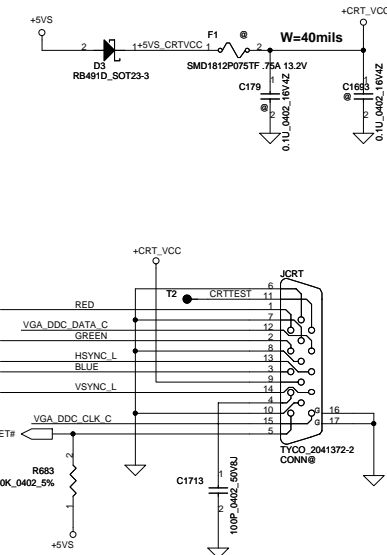
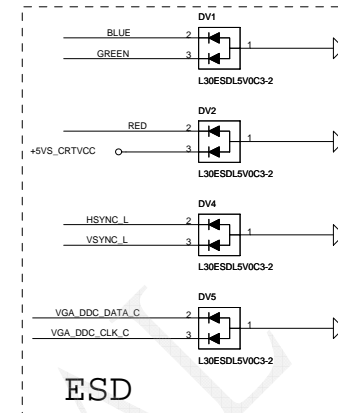
128Mx16 DDR3 *8==>2GB



The schematic diagram illustrates the power management section of the ADALM2000 evaluation board. It shows the following components and connections:

- Power Supply Rails:** +1.5VSG, +5VSG, +VCCP, +1.05VSG, +3VALW, and +3V3.
- Resistors:** R1791 (100K_0402_5%), R1793 (0_0402_5%), R665 (100K_0402_5%), R666 (10K_0402_5%), R192 (10_0603_5%).
- Capacitors:** C333 (0.1U_0402_16V7K), C336 (10L_0603_6.3V6M), C337 (0.01U_0402_25V7K), C338 (1U_0402_6.3V X5R), C339 (10L_0603_6.3V6M), C344 (10L_0603_6.3V6M).
- Diodes:** DIS @ Q81A, DIS @ Q81B, DIS @ Q83A, DIS @ Q83B.
- Transistors:** U30 AO4304L SO8.
- Other Components:** PR05, PR12, PR03, 938L05_T4H0K200204N2, 938L05_T4H0K200204N2.
- Connections:** The diagram shows the connection of various pins (39, 52, 23, 5) to the evaluation board components.

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[illegible]

LCD POWER CIRCUIT

The circuit diagram illustrates the power supply and backlight control for an LCD. Key components and their values are as follows:

- Input Filtering:** C192 (0.1uF, 0.0402, 16V4Z) and C104 (0.1uF, 0.0402, 16V4Z) are used for input filtering.
- Voltage Divider:** R119 (100.0805, 5%) is used to divide the input voltage.
- MOSFET Driver:** Q32A (2N7002DW-7-F, SOT363-6) is the MOSFET driver.
- MOSFET:** Q32B (2N7002DW-7-F, SOT363-6) is the MOSFET.
- Diode:** D1 (1N4148, 5VSR) is a diode.
- Resistors:** R121 (47K, 0.402, 5%), R123 (220K, 0.402, 1%), R130 (100K, 0.402, 5%), R182 (0.402, 5%), R122 (10K, 0.402, 5%), and RV42 (33.0402, 5%) are used for various functions.
- Panel Backlight Control:** The circuit includes a BKOFF# signal and a diode (D1) for backlight control.

LCD POWER CIRCUIT

The circuit diagram illustrates the power supply and backlight control for an LCD. Key components and their values are as follows:

- Input Filtering:** C192 (0.1uF, 0.0402, 16V4Z) and C104 (0.1uF, 0.0402, 16V4Z) are used for input filtering.
- Voltage Divider:** R119 (100.0805, 5%) is used to divide the input voltage.
- MOSFET Driver:** Q32A (2N7002DW-7-F, SOT363-6) is the MOSFET driver.
- MOSFET:** Q32B (2N7002DW-7-F, SOT363-6) is the MOSFET.
- Diode:** D1 (1N4148, 5VSR) is a diode.
- Resistors:** R121 (47K, 0.402, 5%), R123 (220K, 0.402, 1%), R130 (100K, 0.402, 5%), R182 (0.402, 5%), R122 (10K, 0.402, 5%), and RV42 (33.0402, 5%).
- Panel Backlight Control:** The circuit includes a BKOFF# signal and a diode (D1) for backlight control.

Panel PWM Control

3V3

R117
4.7K_0.402_5%

INV/TPWM

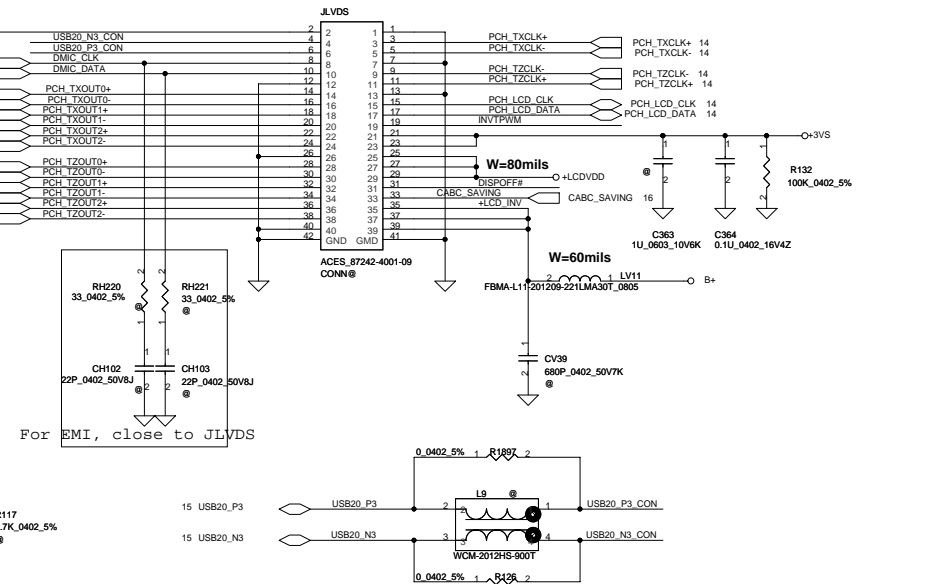
R1864
0.402_5%

PR05

39 EC_INV_PWM

14 PCH_INV_PWM

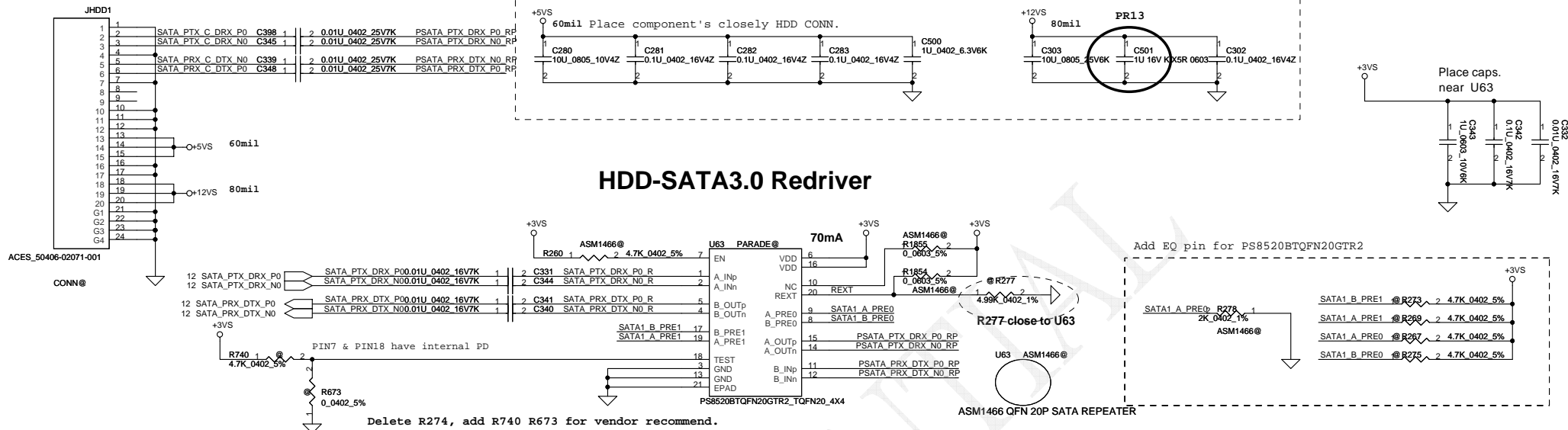
Security Class



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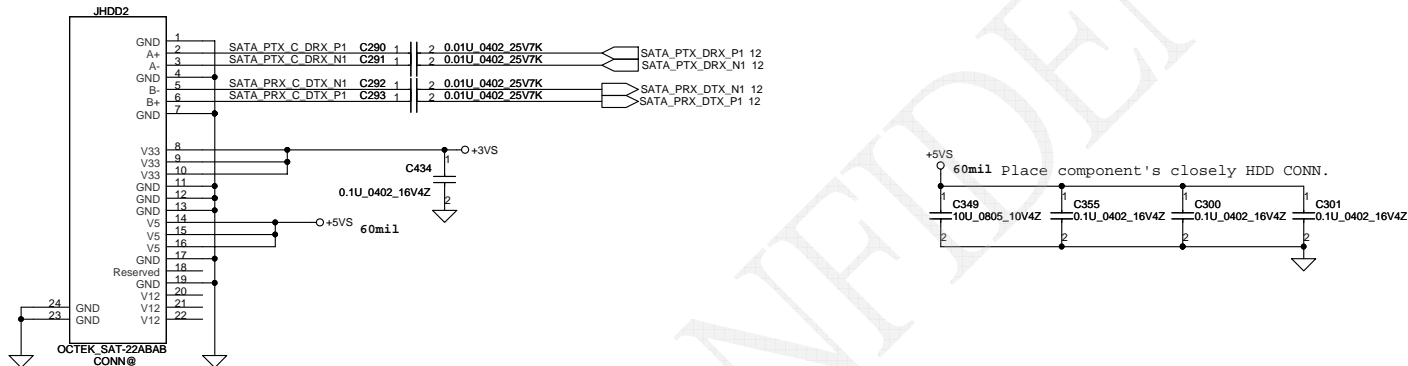
HDD1

SATA HDD 3.5" Conn.

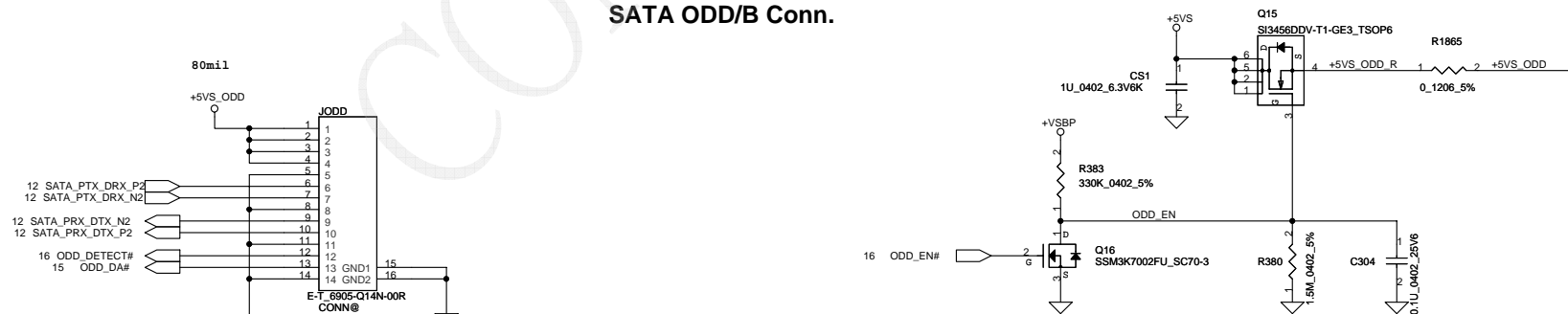


HDD2

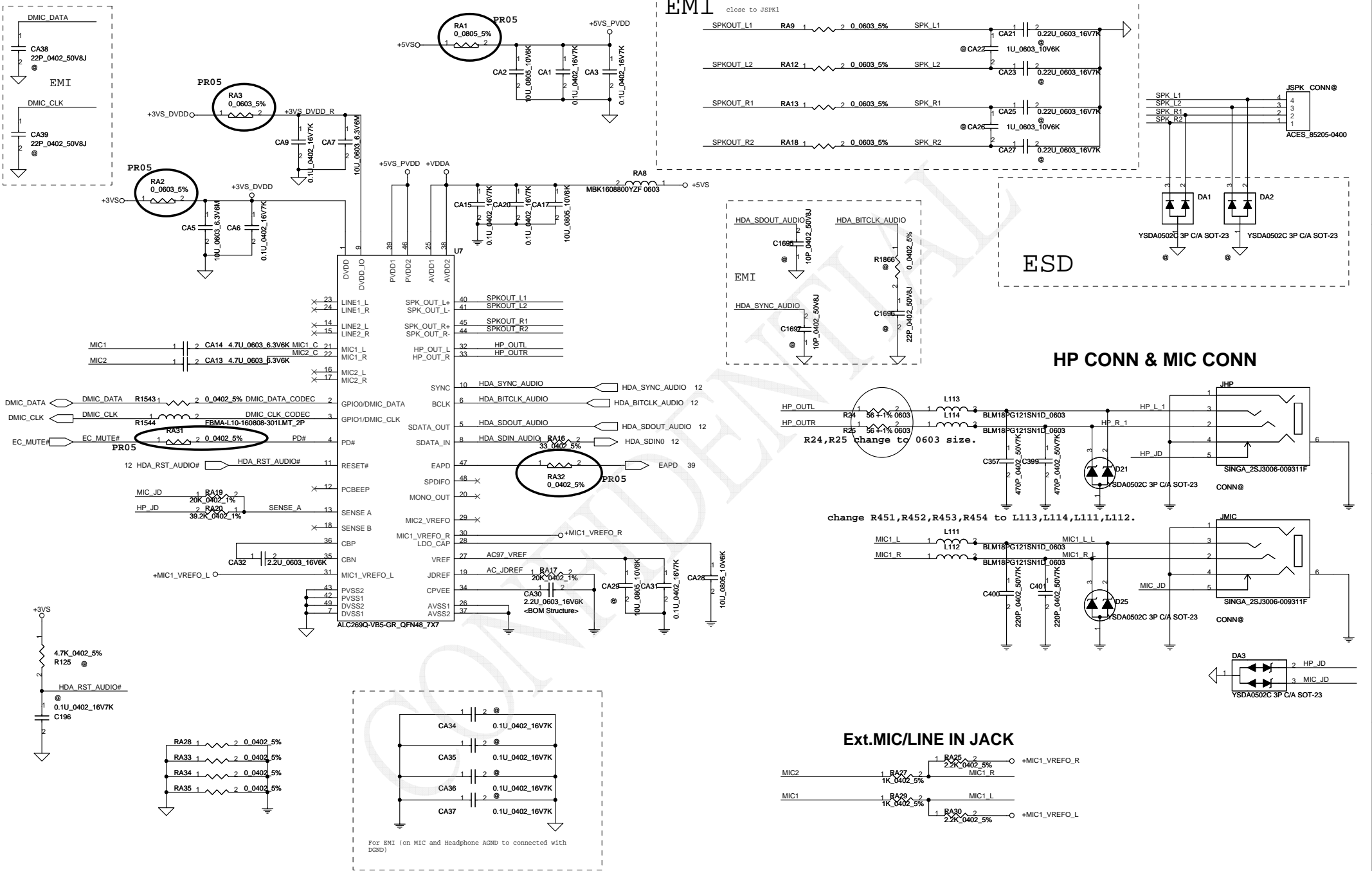
SATA HDD 2.5" Conn.



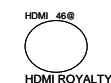
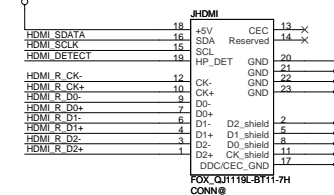
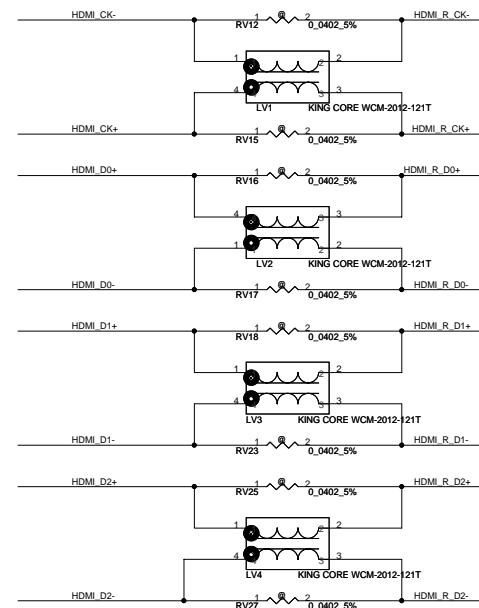
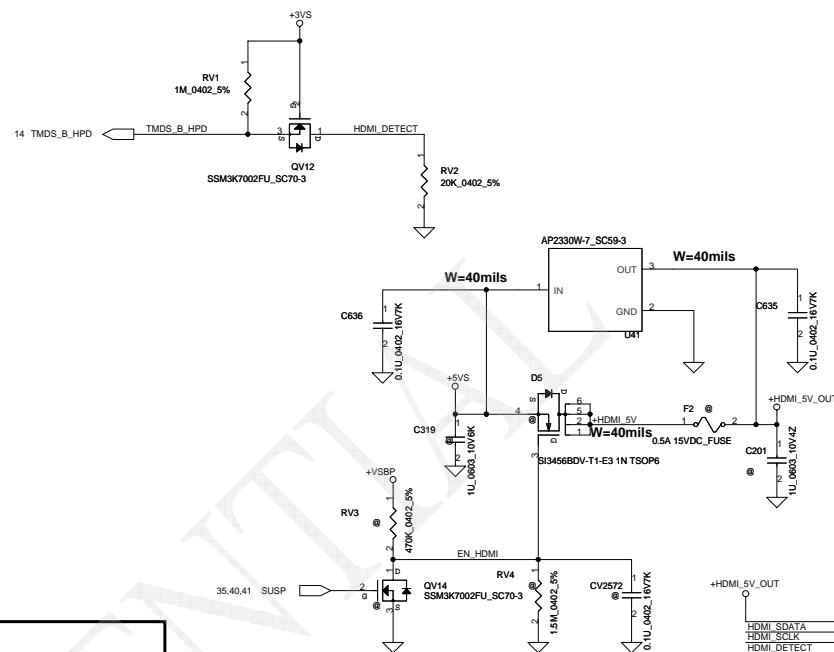
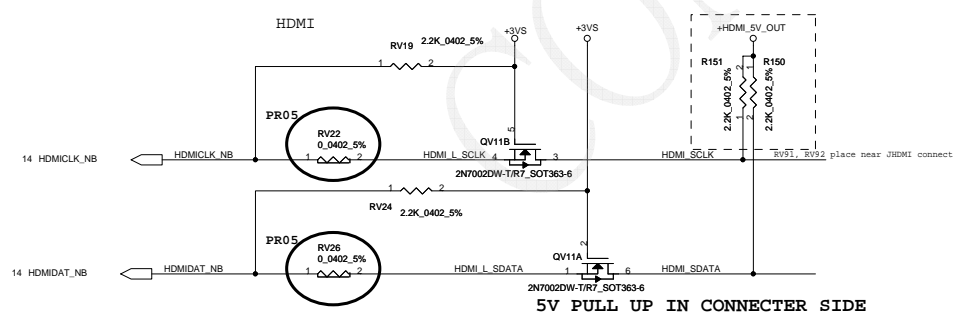
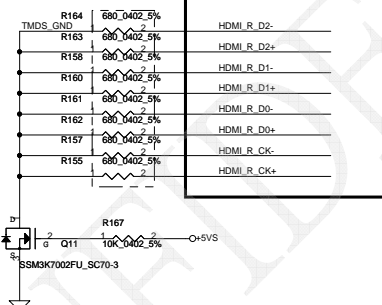
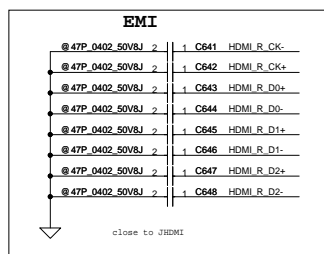
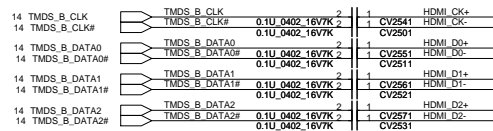
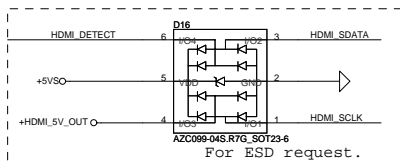
SATA ODD/B Conn.



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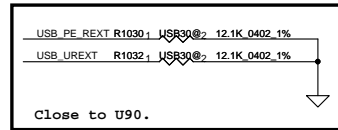
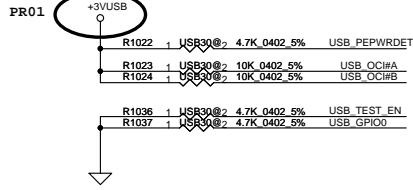
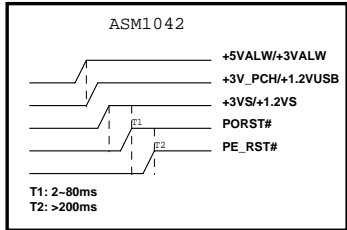


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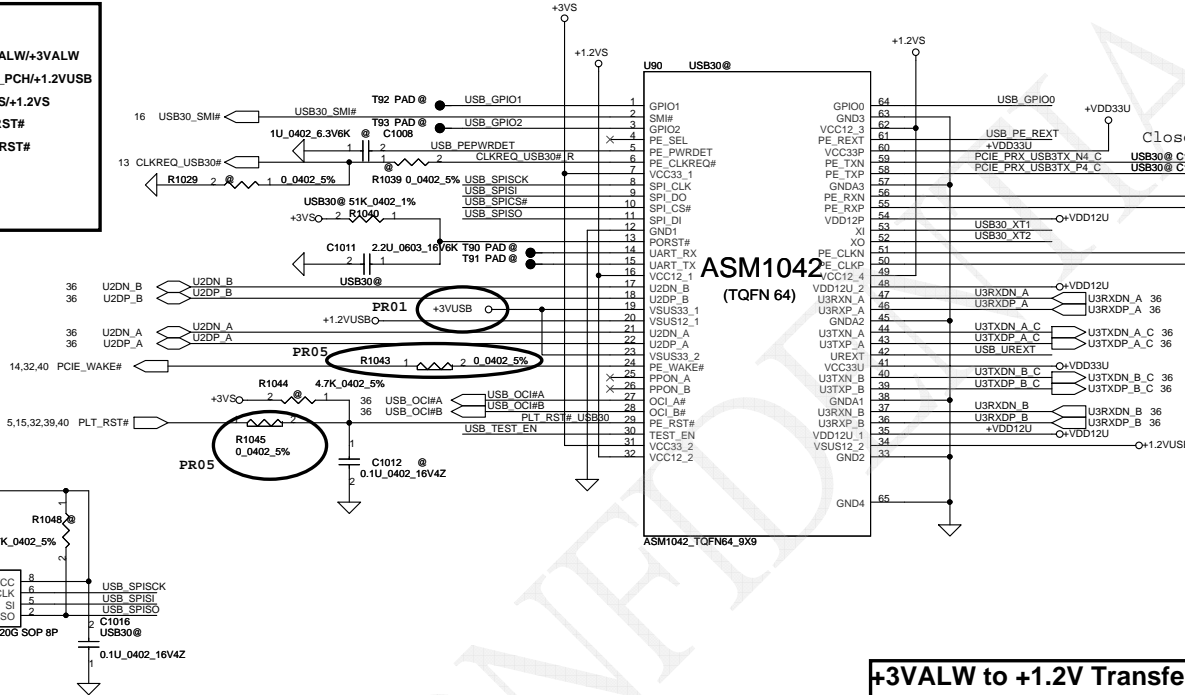
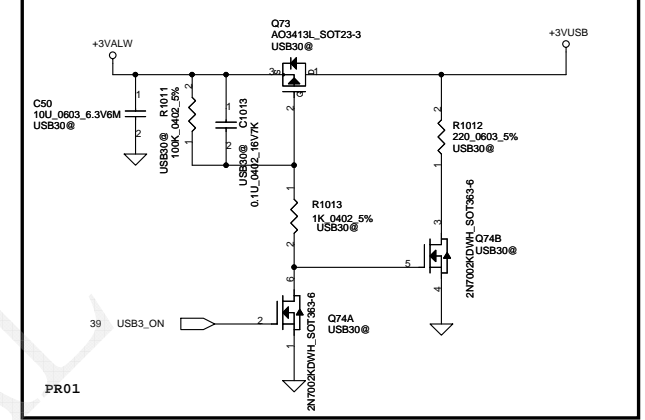


	S3	S4/S5
+3V_PCH	V	X
+3VS	X	X
+1.2VUSB	V	X
+1.2VS	X	X

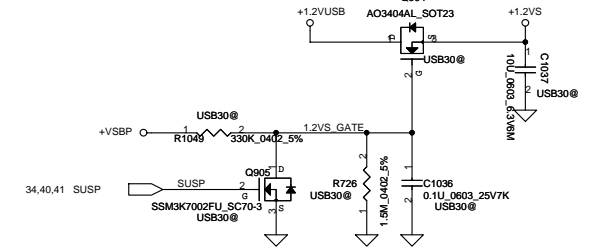
Power Sequence

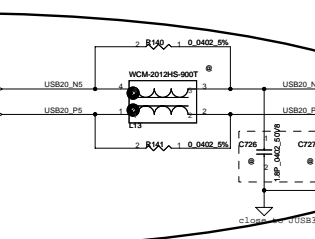
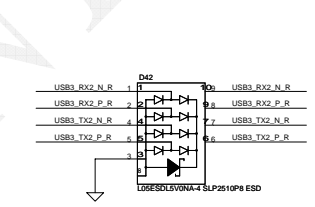
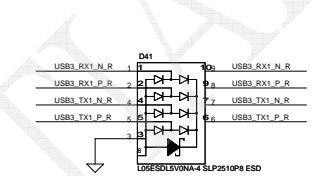
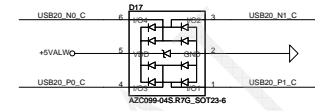
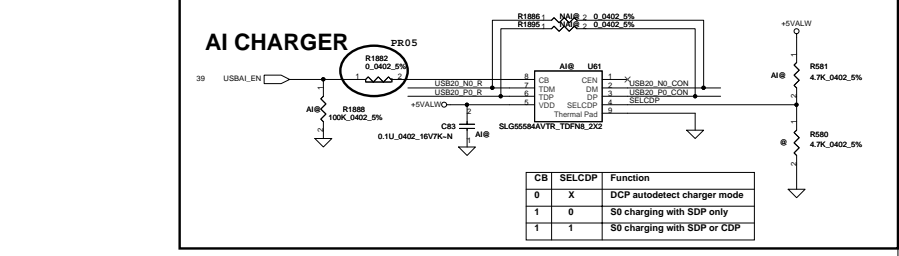
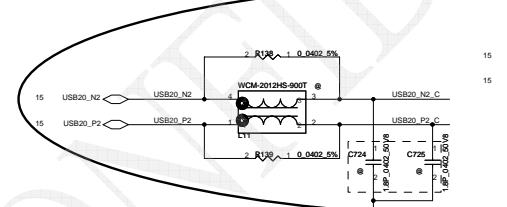
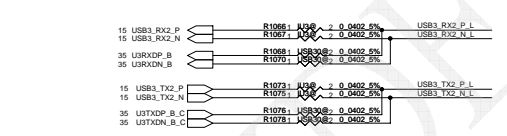
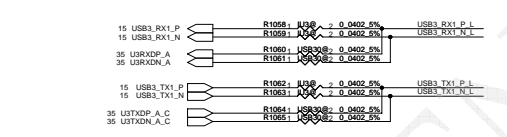
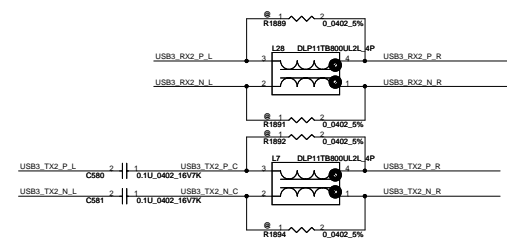
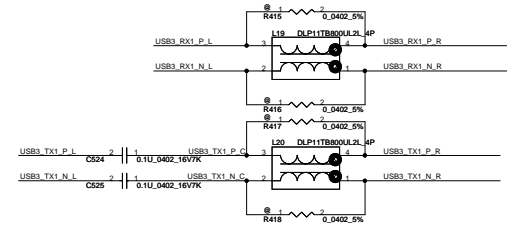
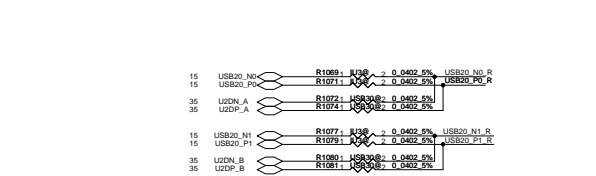
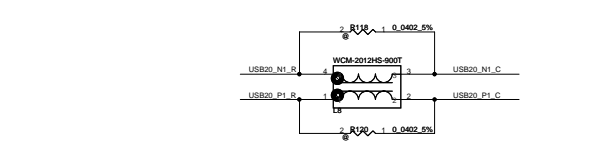
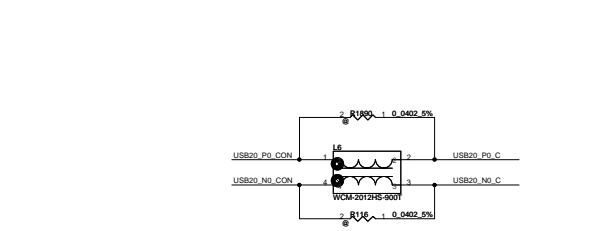
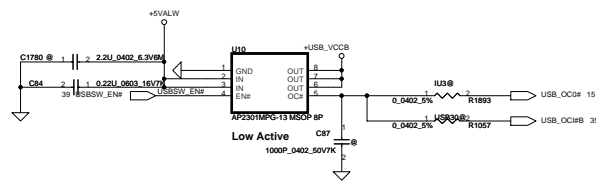
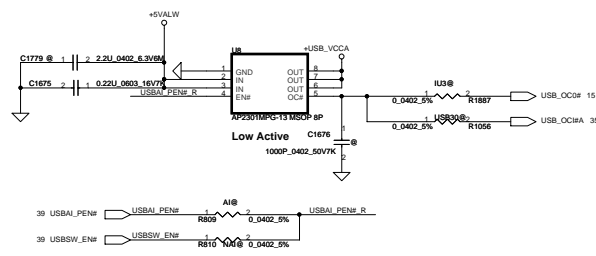


+3VALW to +3VUSB Transfer

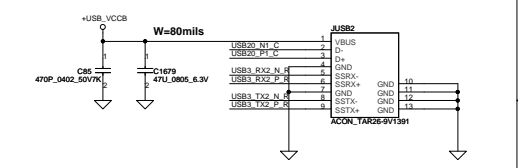
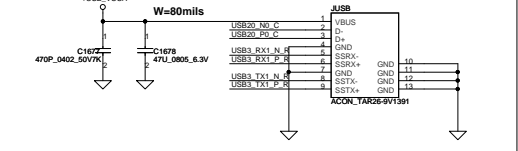


+1.2VUSB TO +1.2VS

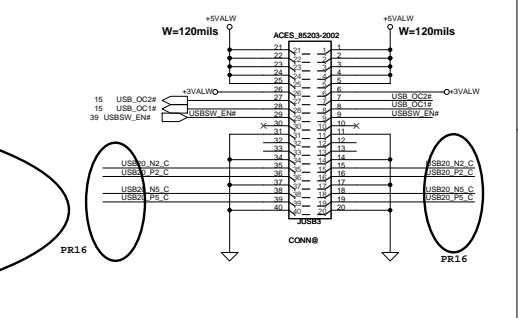




charger port: left side & near user

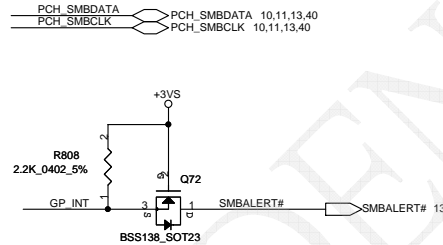
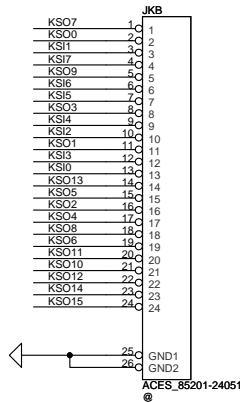
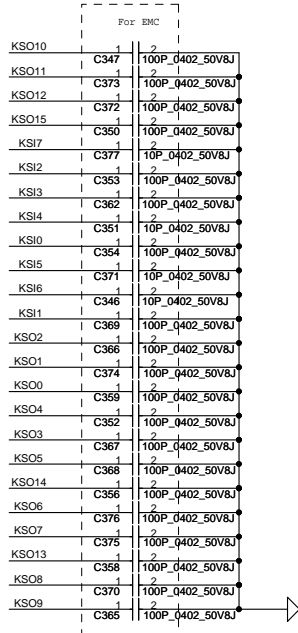


USB Right USB X 2

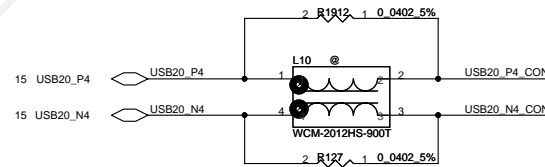
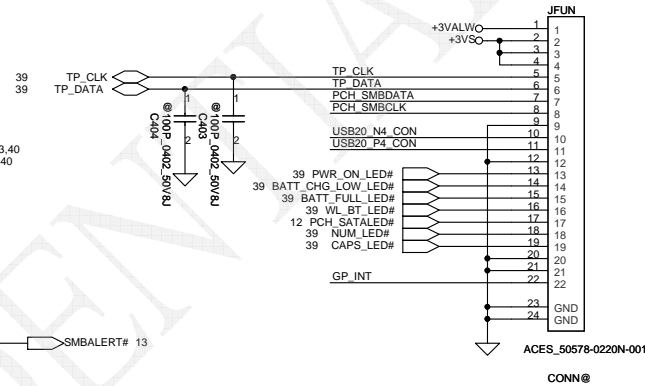


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				4019C7	B
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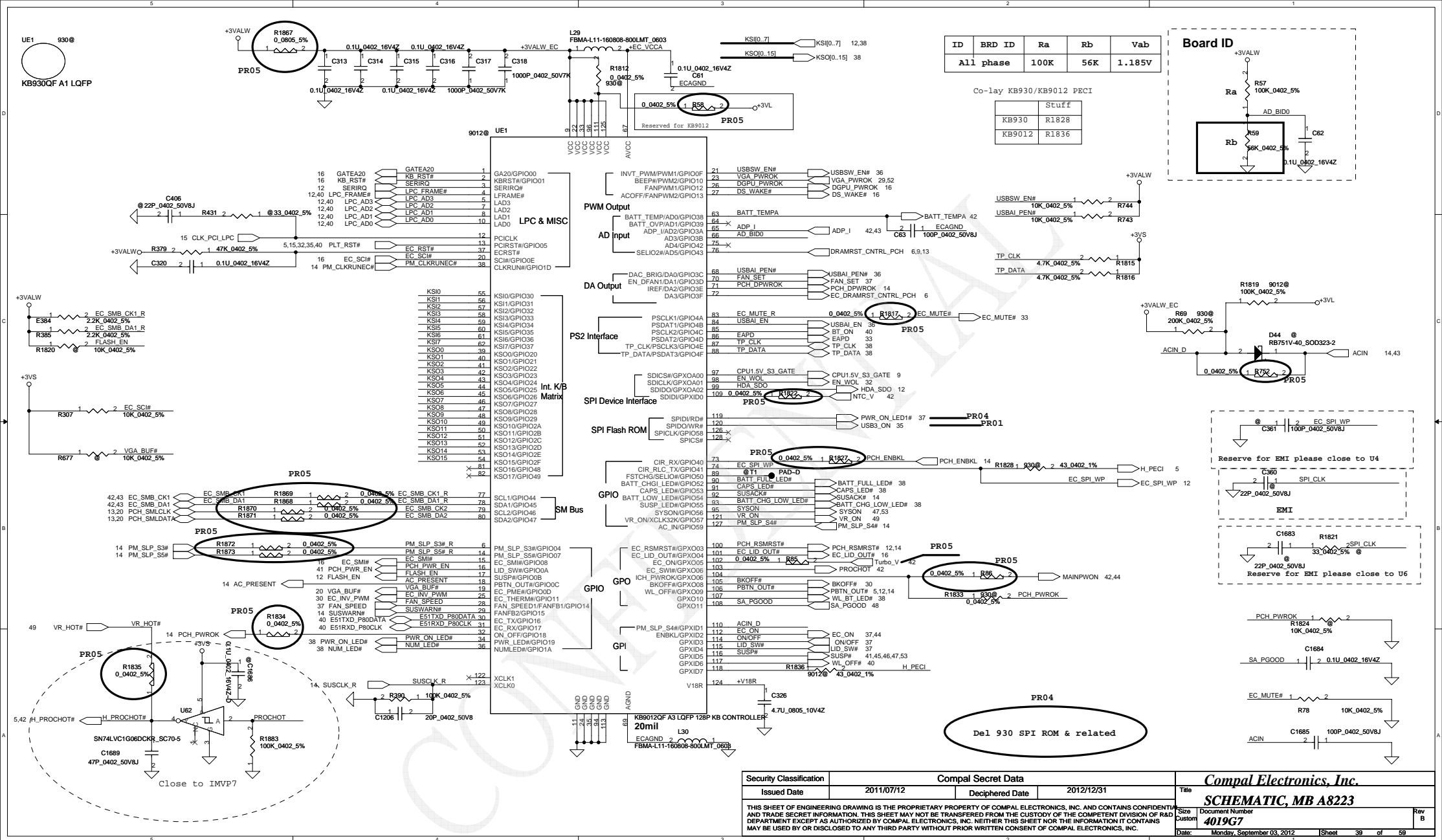
INT_KBD Conn.

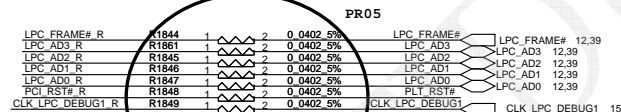
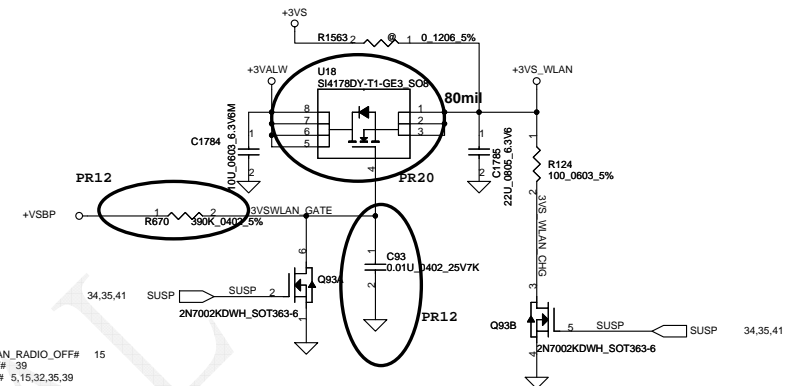


Touch pad & LID & Card Reader & LED small board Connector



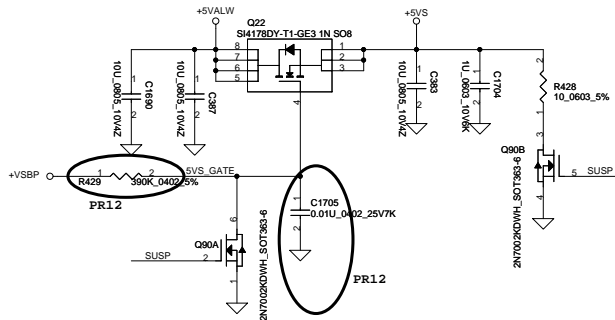
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				Date:	Monday, September 03, 2012
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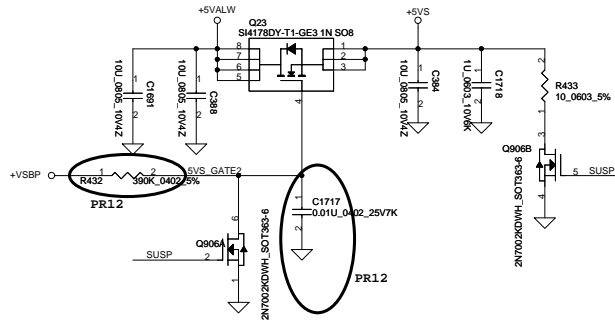


	Compal Electronics, Inc.
Title	SCHEMATIC, MB A8223

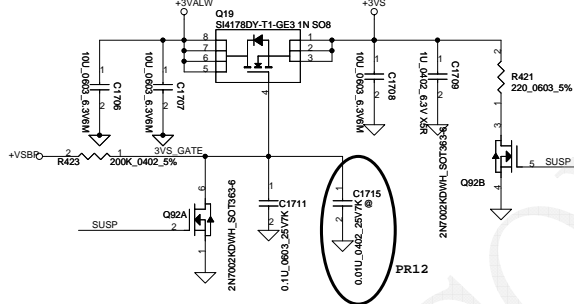
+5VALW TO +5VS



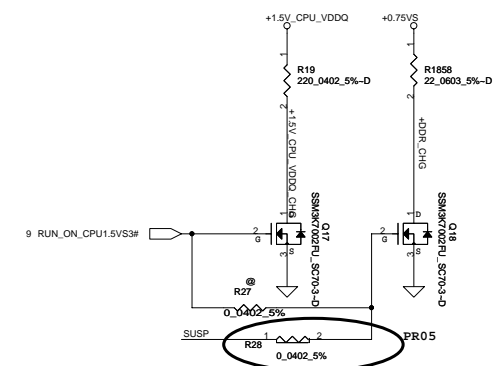
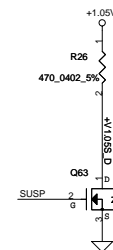
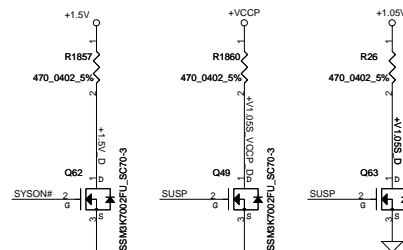
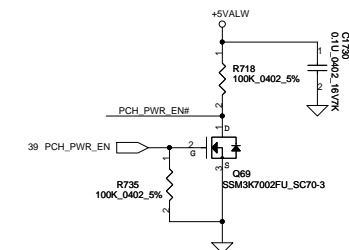
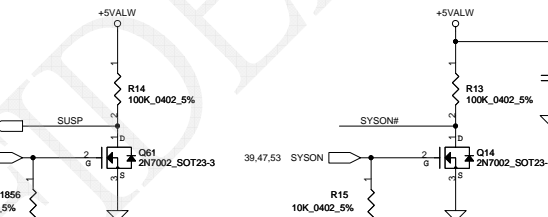
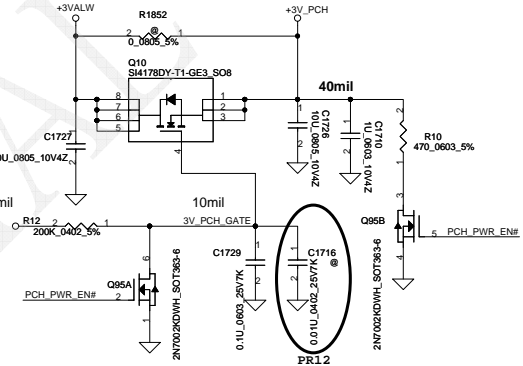
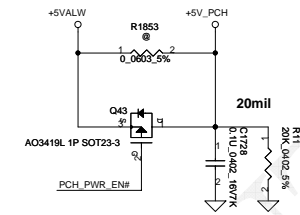
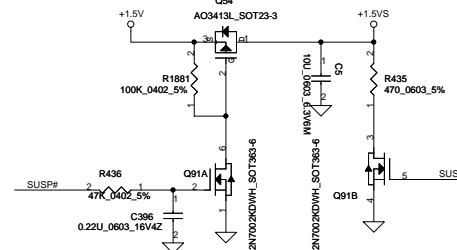
+5VALW TO +5VS (close to HDD1)



+3VALW TO +3VS

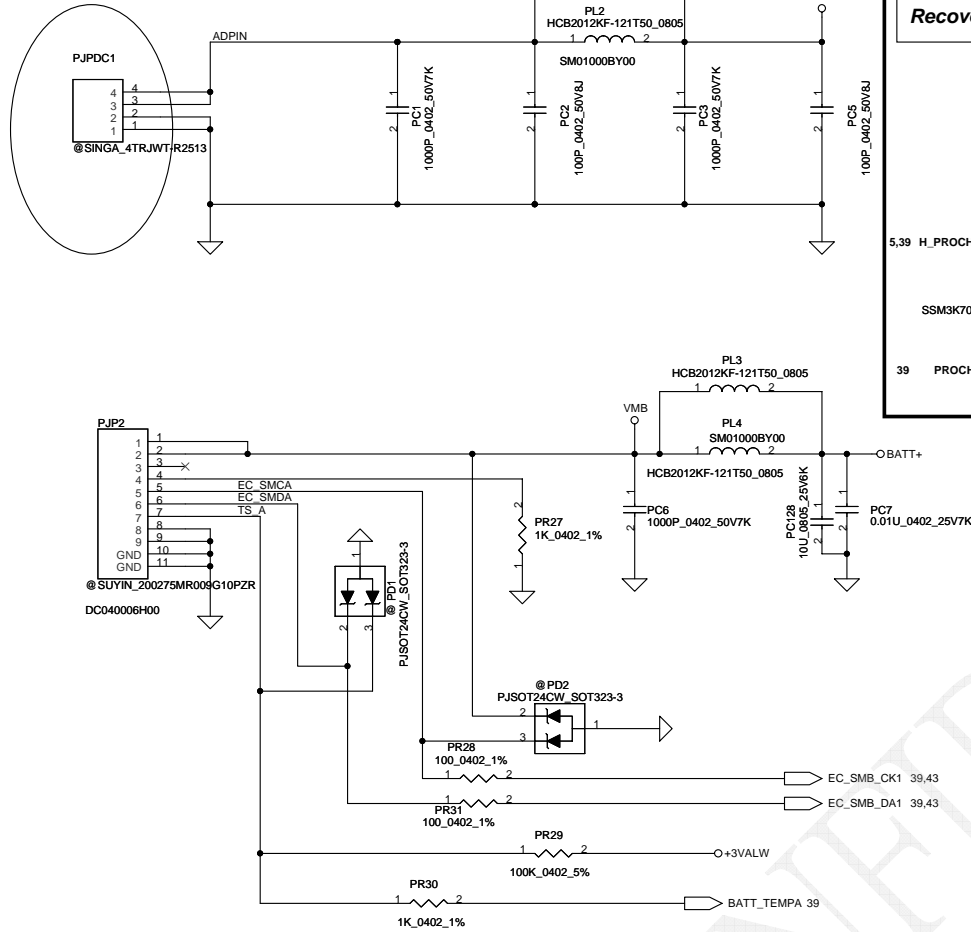


+1.5V TO +1.5VS

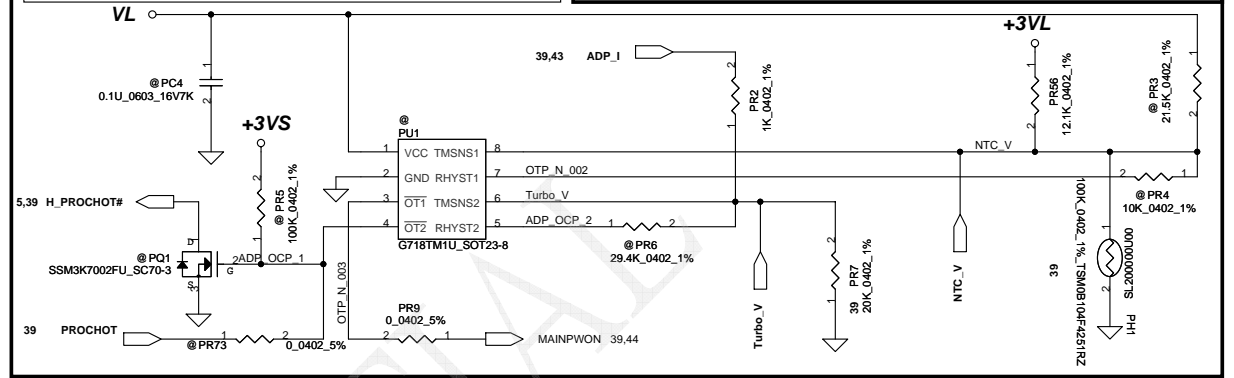


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DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME

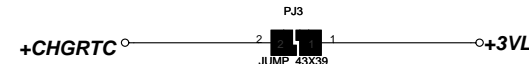
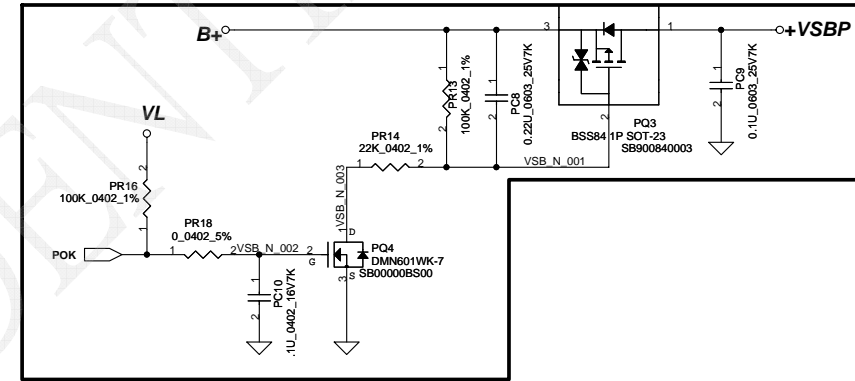


PH1 under CPU bottom side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C



For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

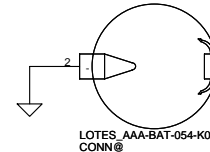
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR56
PH1, PR2, PQ1, PR7,PQ15,PR73,PR56



RTC Battery

PBJ1

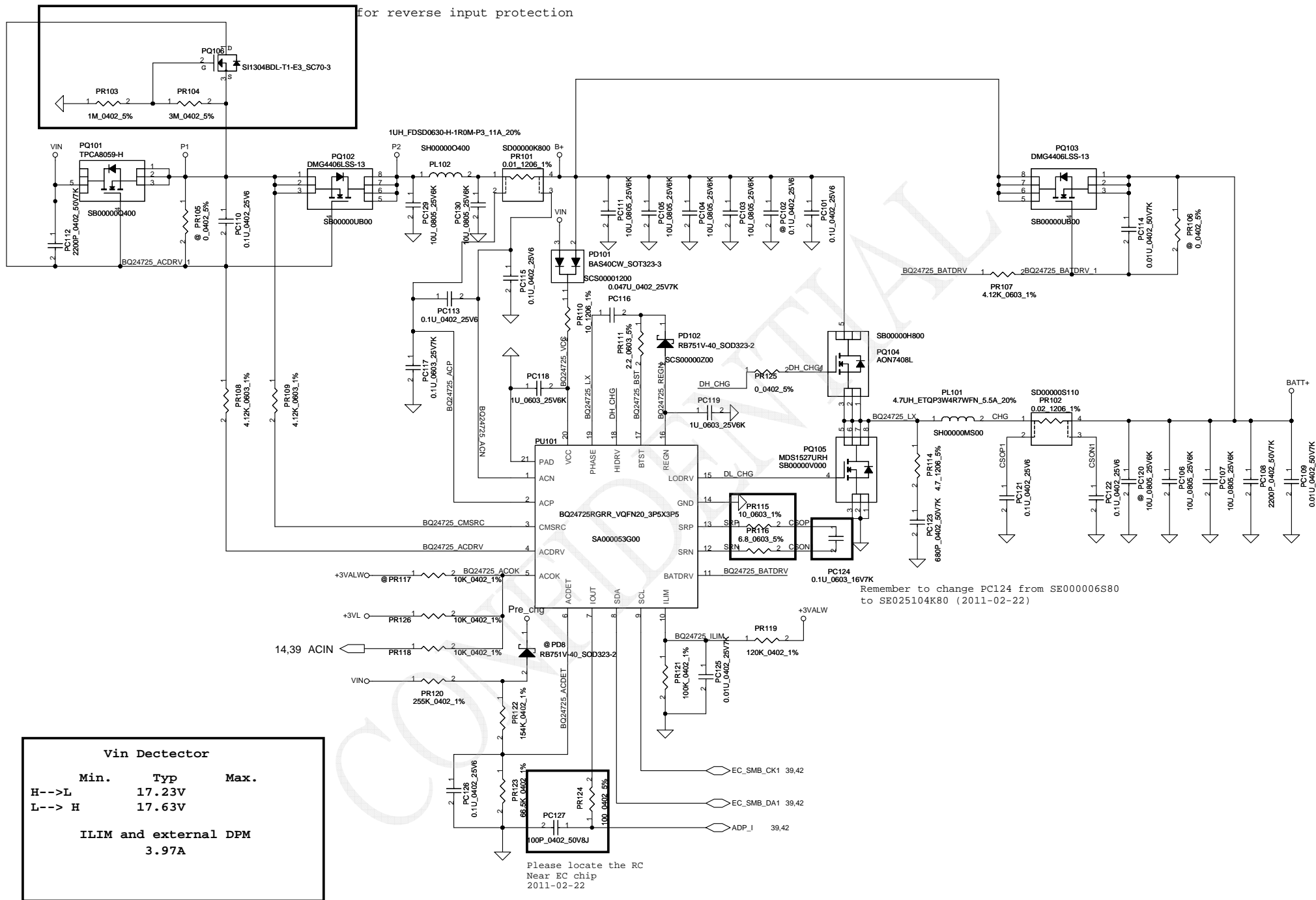
Must close PBJ1

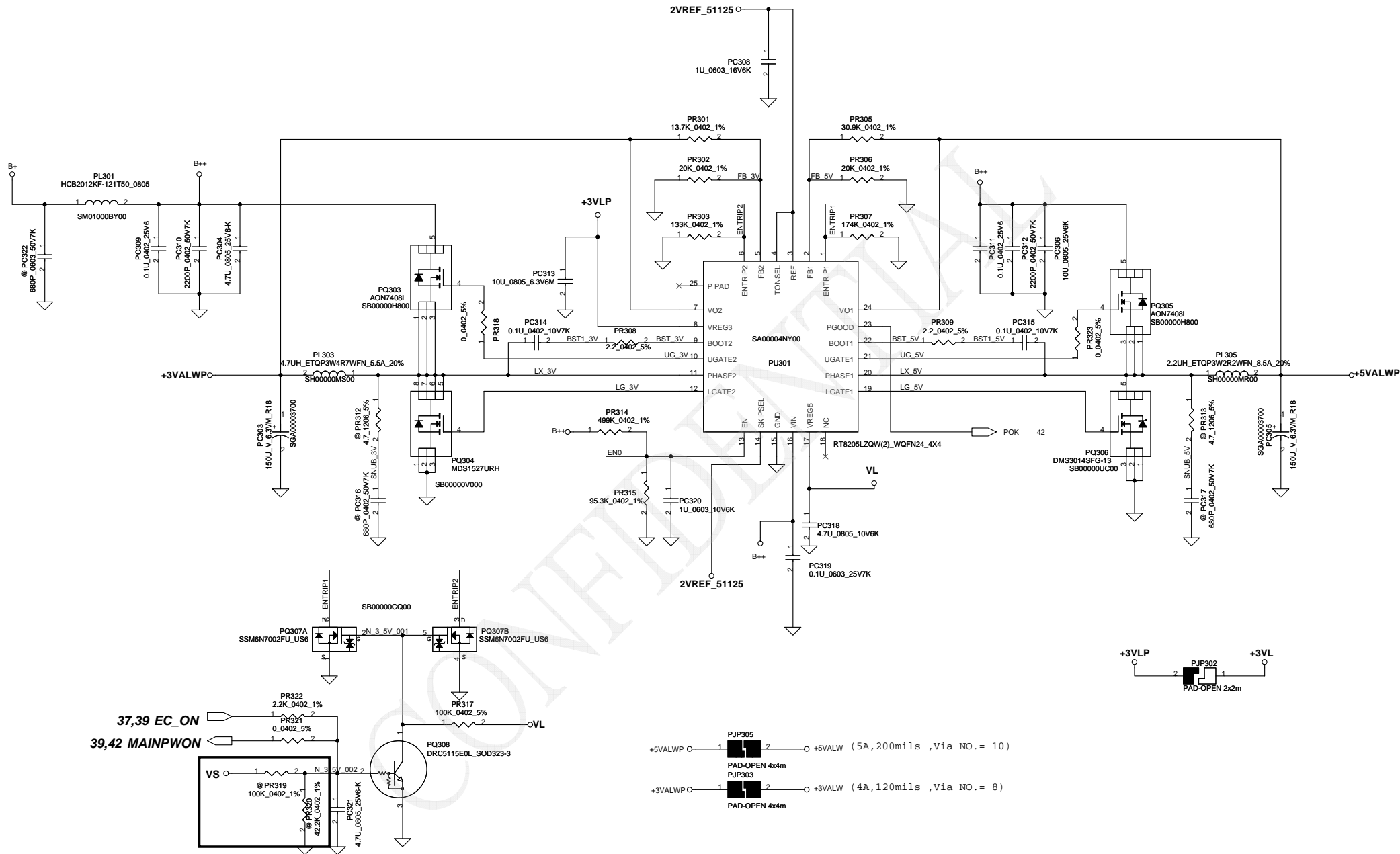


Change RTC For Cost Down
SP07000H700

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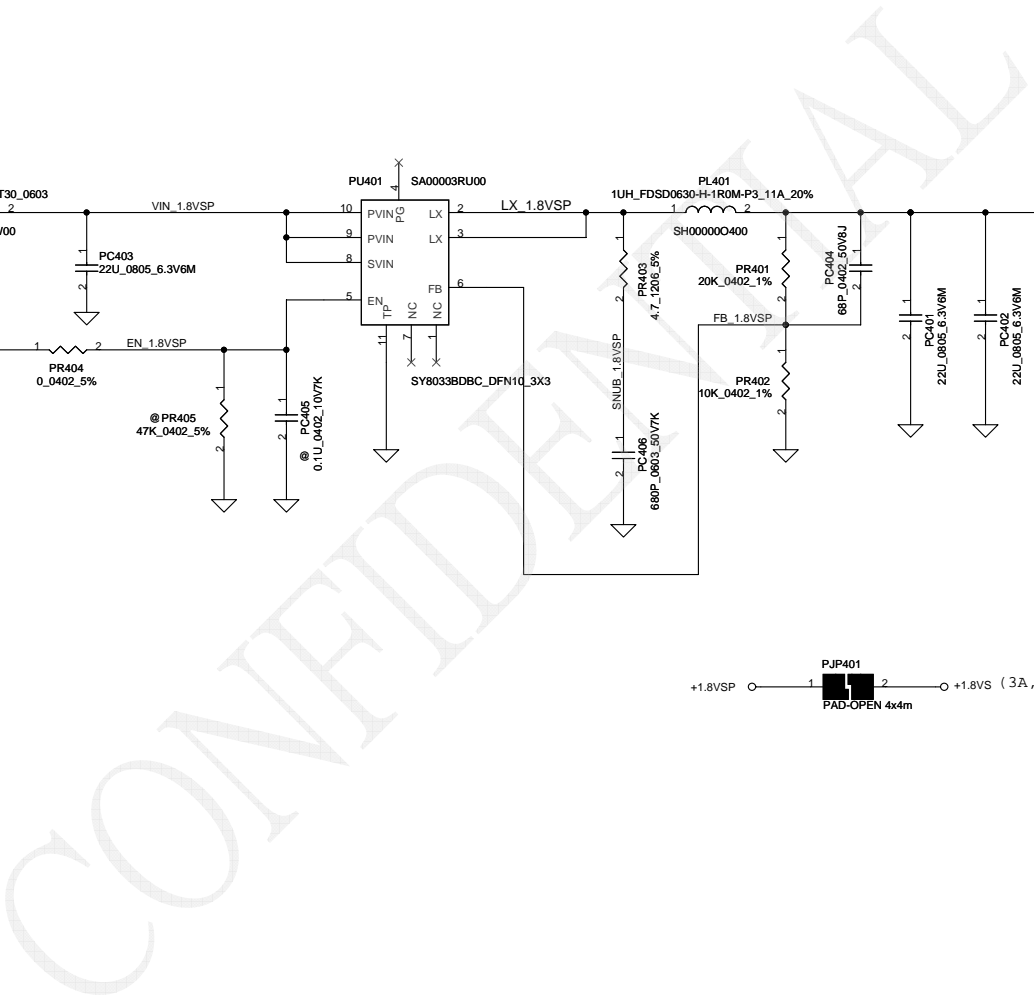
For KB9012 --> Remove all 51_ON# circuit



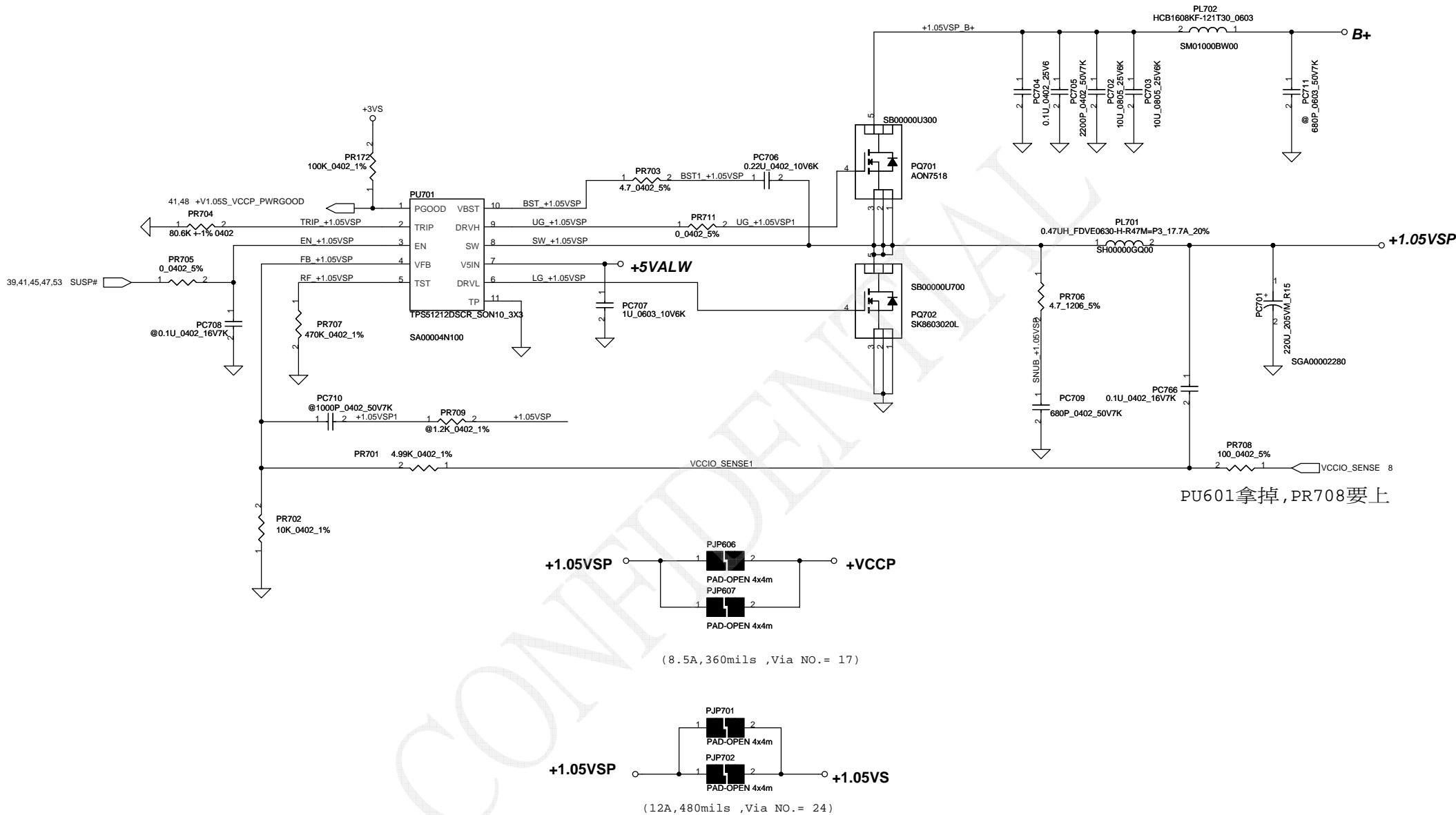


For KB930 --> Keep PR319, Remove PR322
 For KB9012 (Red square) --> Remove PR319
 Keep PR322

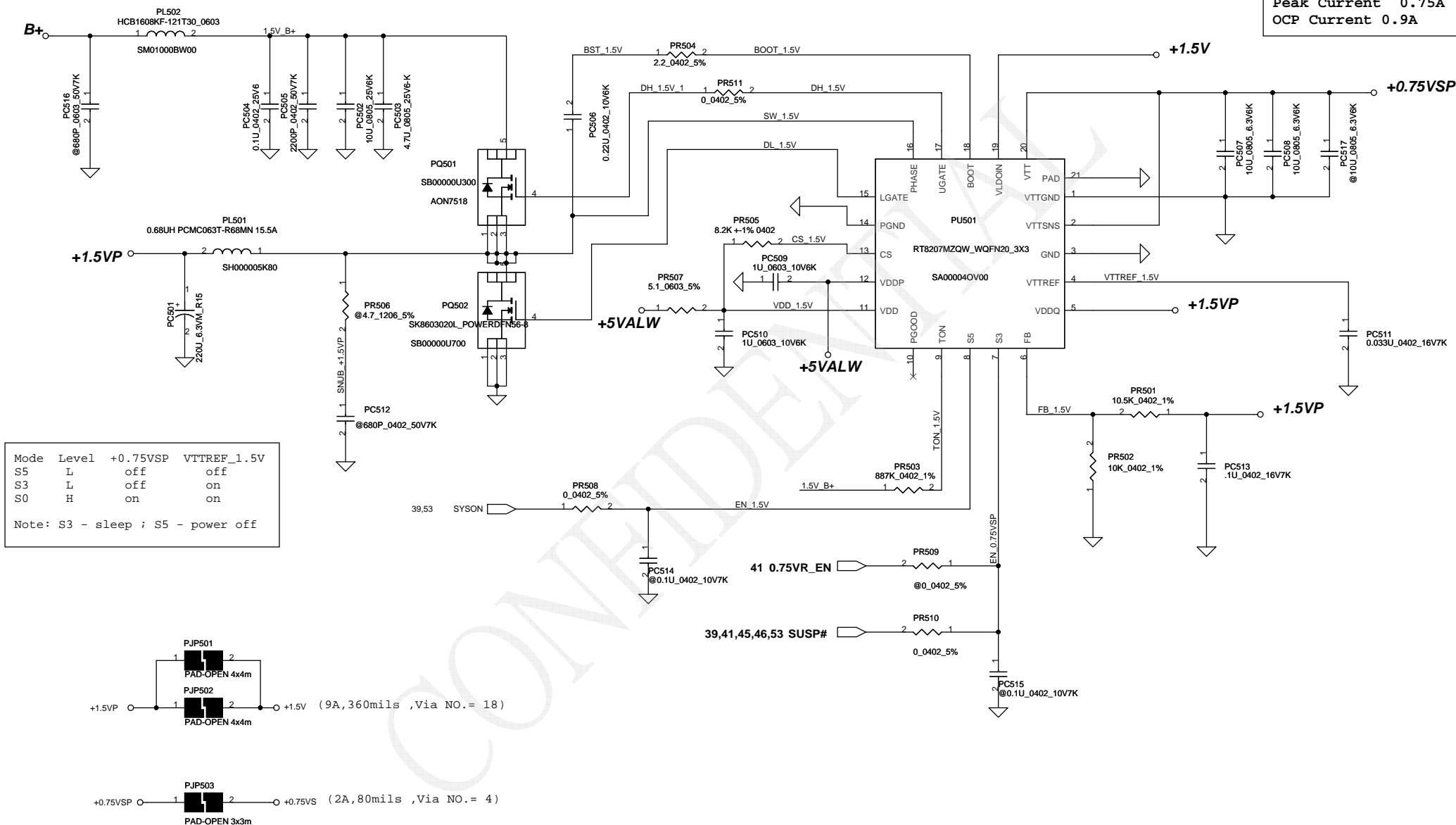
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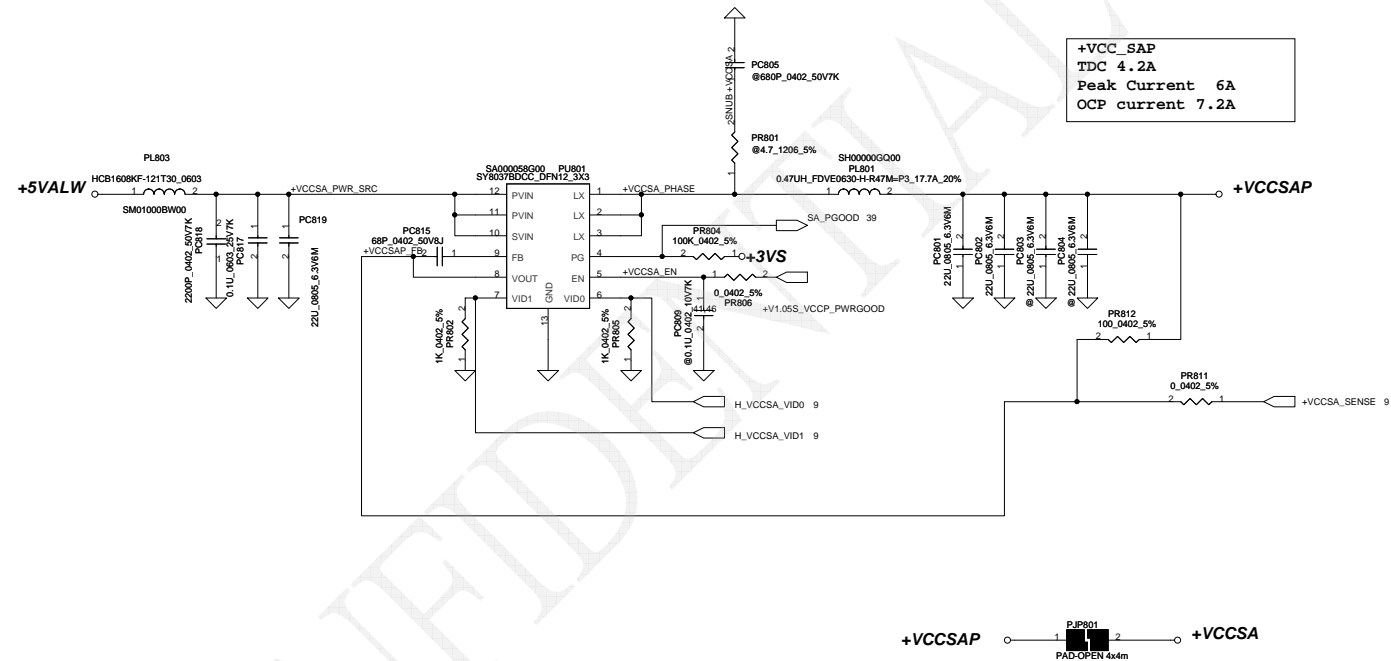


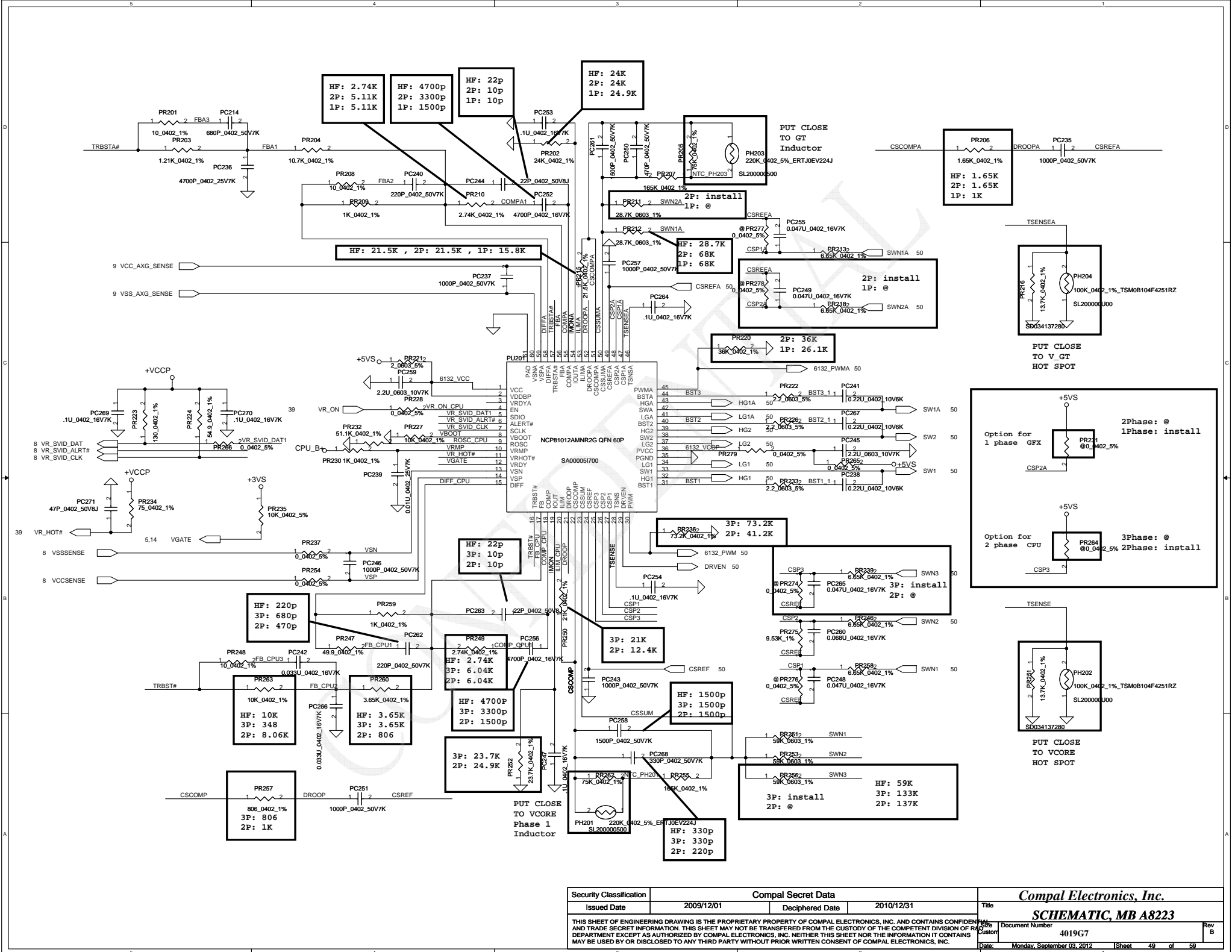
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The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network





+VCC_CORE

+VCC_CORE

+VCC_GFXCORE_AXG

Below is 458544_CRV_PDDG_0.5 Table 5-8.

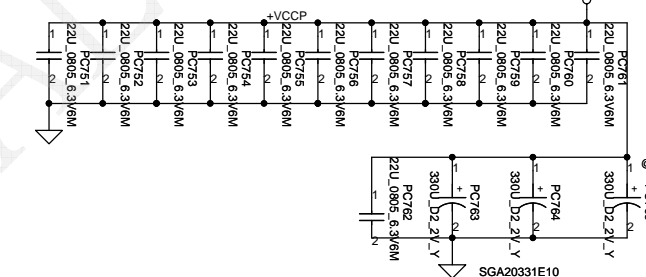
Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+VCC_CORE

+VCC_GFXCORE_AXG

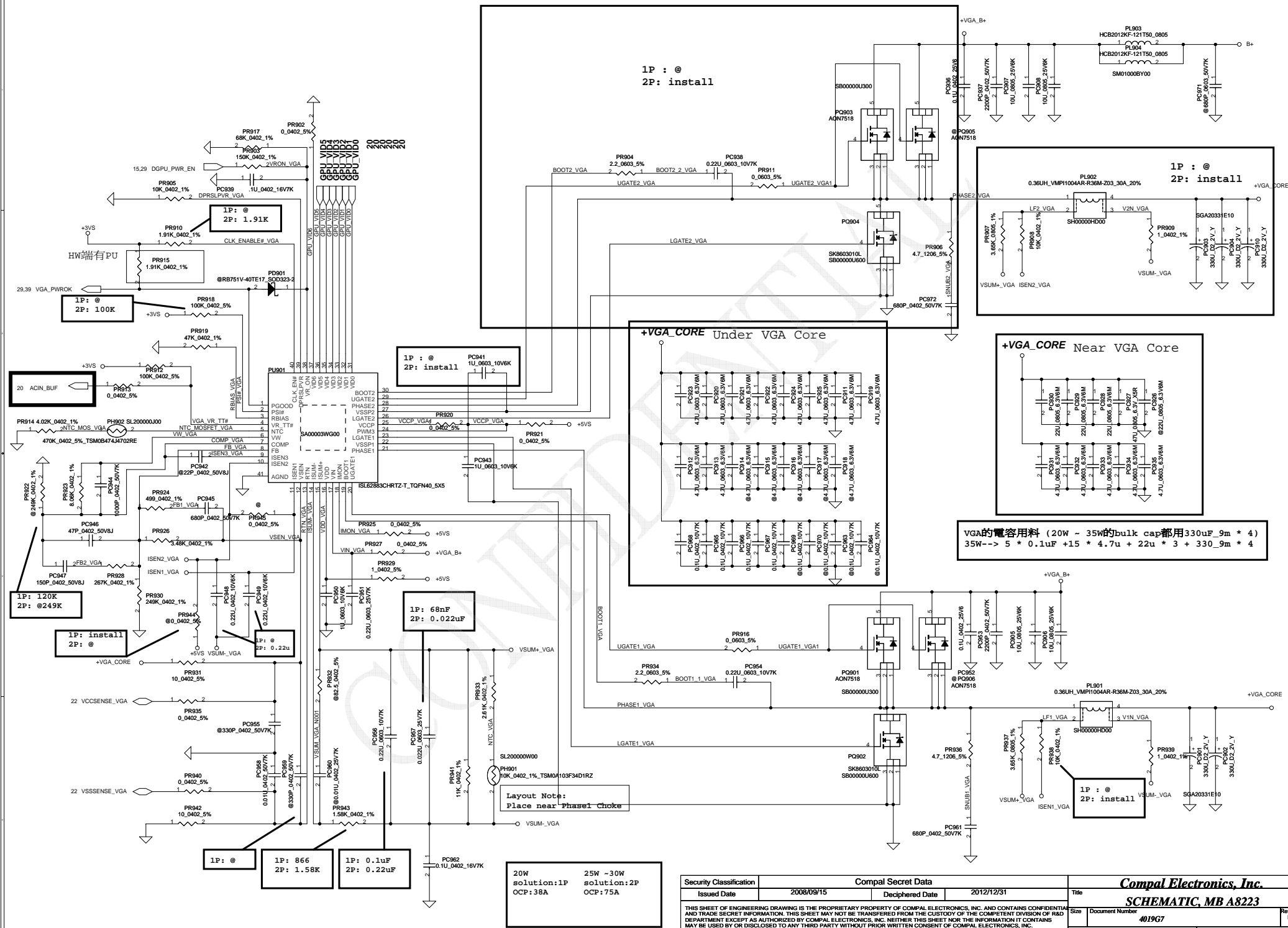
+VCCP

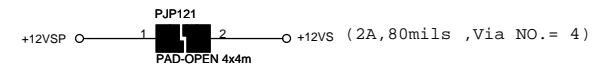
+VCC_CORE



Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

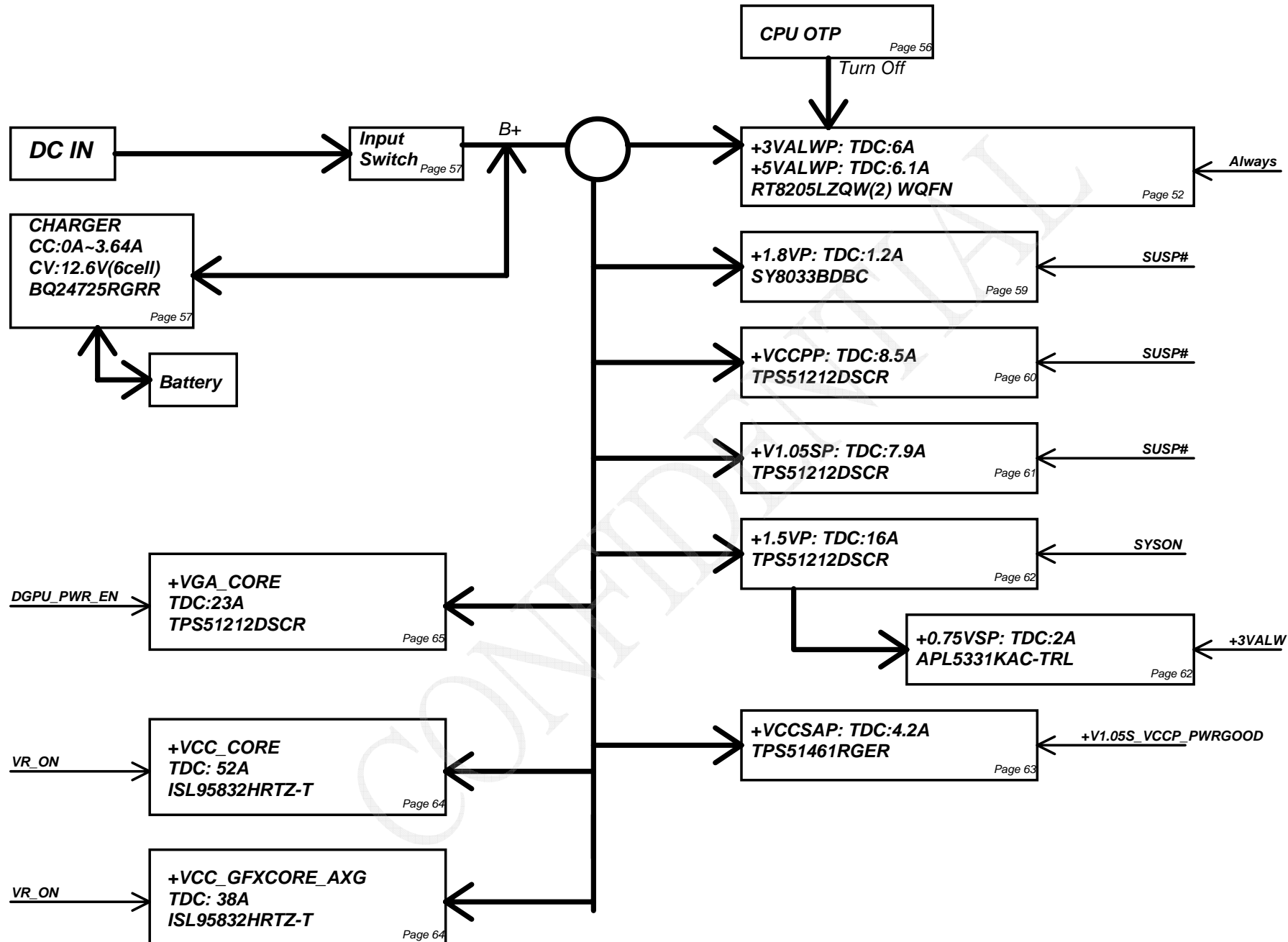
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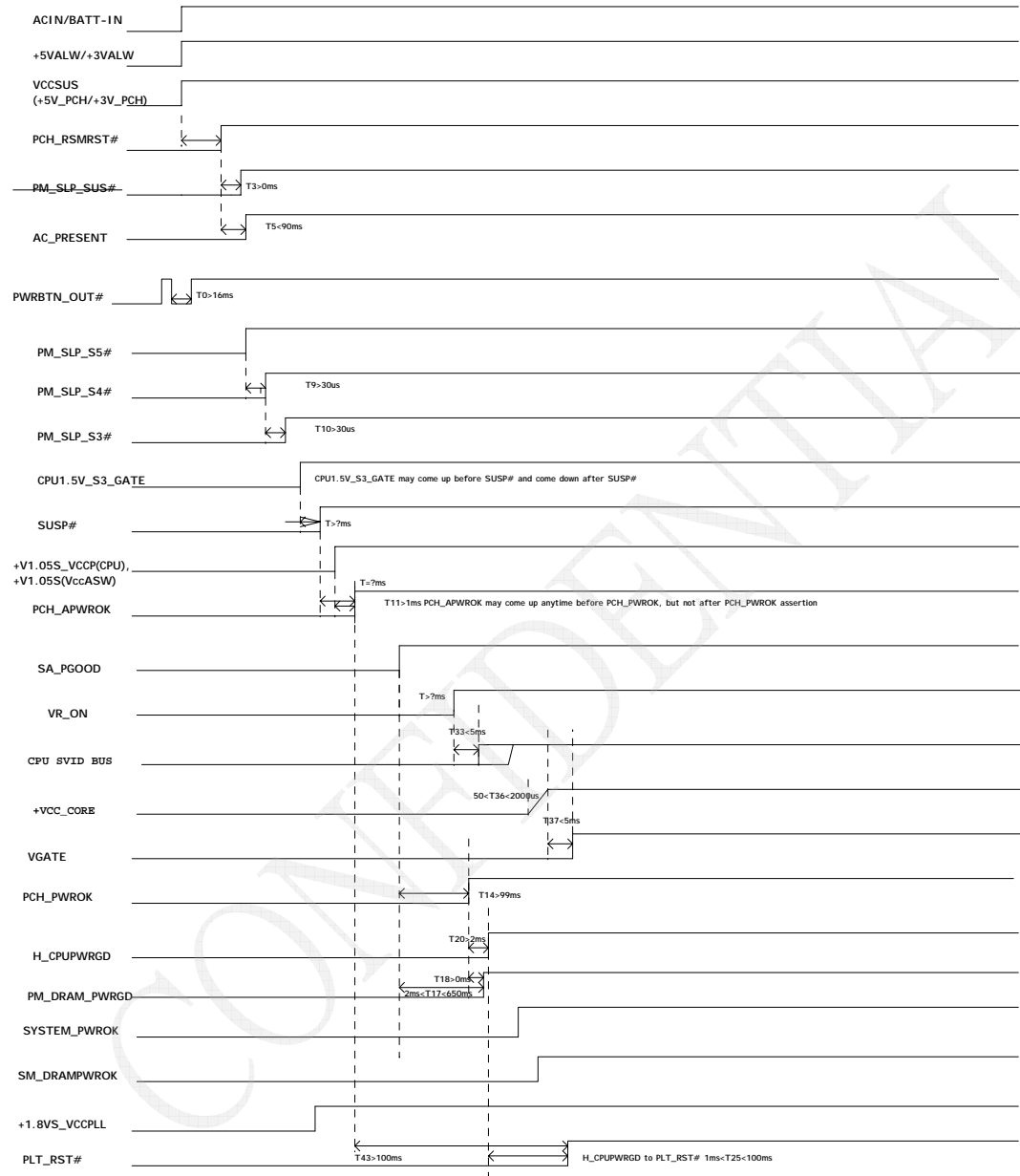
Power block



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Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

HW Version Change List (P. I. R. List) Page 1/3

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
ER01	02#	Block Diagram	0830	ShouYi	Modify the external USB 3.0 page.		0.2
ER03	35#	PCIe USB3.0 ASM1042	0830	ShouYi	Add External USB3.0 controller circuit.		0.2
ER04	13#	PCH SMBUS,CLK	0830	ShouYi	Add External USB3.0 circuit of PCIE Port4	Modify PCIE-Port4 of PCH circuit.	0.2
ER05	13#	PCH SMBUS,CLK	0830	ShouYi	Add circuit of CLK port3 for external USB3.0	Modify CLK port3 of PCH circuit.	0.2
ER07	16#	CPU RSVD,CFG	0831	ShouYi	Add USB30_SMI# for external USB3.0	Add USB3.0 SMI signal.	0.2
ER08	40#	MINI CARD	0906	ShouYi	Can't boot.	Stuff 0.1uF of C93.	0.2
ER09	07#	CPU RSVD,CFG	0913	ShouYi	For improve layout space.	Add CLK_RES_ITP and CLK_RES_ITP# to TP.	0.2
ER10	13#	PCH SMBUS,CLK	0913	ShouYi	For improve layout space.	Del RH19,RH20,R1758,R1759.	0.2
ER11	37#	FAN/PWRBTN/PCB PN	0914	ShouYi	For mechanic's requirement.	H7 change from 3P3 to 4P1.	0.2
ER12	13#	PCH PCIE,SMBUS,CLK	0922	ShouYi	Reserve R1899 to GND		0.2
ER13	35#	PCIe USB3.0 ASM1042	0922	ShouYi	Modify USB3.0 circuit.	Modify +1.2VUSB to 1.2VS circuit and swap signals. Change R1040 to 47K and ADD R1029 to GND.	0.2
ER14	18#	PCH PWR(7/8)	0922	ShouYi	For support WLAN wake up.	Reserve R381 to +3VALW.	0.2
ER15	05#	CPU PM,XDP,CLK	0922	ShouYi	For improve layout space.	Delete T65,T66.	0.2
ER16	35#	PCIe USB3.0 ASM1042	0922	ShouYi	Delete USB3.0 delay PORST circuit.		0.2
ER17	41#	DC/DC Interface	0922	ShouYi	Modify Q54 P/N.	Change Q54 to SB934130020.	0.2
ER18	29#	VGA DC/DC Interface	0922	ShouYi	Modify U17 P/N and Reserve R1898.		0.2
ER20	14#	PCH DMI,FDI,PM,GFX, DP	0923	ShouYi	HDMI Detect modify.	Delete R213.	0.2
ER21	13#	PCH SMBUS,CLK	0923	ShouYi	For improve +3VS leakage voltage on S3/S4/S5.	Delete Q33 circuit.	0.2
ER22	13#	PCH PCIE,SMBUS,CLK	0923	ShouYi	For 48M CLK EA fail.	Change R1797 from 0 ohm to 22 ohm.	0.2
ER23	36#	USB2.0 USB	0923	ShouYi	Reserve 0 ohm for un-discharge.	Reserve R1886 and R1895.	0.2
ER24	39#	EC KB930	0923	ShouYi	SMBus circuit modify.	Delete R386, R387.	0.2
ER25	37#	FAN/PWRBTN/PCB PN	0927	ShouYi	For LID signal floating.	Add R578 to +3VALW.	0.2
ER26	29#	VGA DC/DC Interface	0927	ShouYi	For DGPU Power Sequence	Change R1793 to 0 ohm and C333 to unstuff.	0.2
ER27	07#	CPU RSVD,CFG	0928	ShouYi	Delete T70,T71 (no need)		0.2
ER28	31#	HDD,ODD/B Conn	0928	ShouYi	For co-lay ASM1466.	Delete R265,R272,R270. Change R278 to 2K and modify to ASM1466@. Reserve R1854,R1855 to +3VS.	0.2
ER29	35#	PCIe USB3.0 ASM1042	0928	ShouYi	Remove no use the signals.	Delete R1021,R1033,R1034,R1028,R1031.	0.2
ER30	39#	EC KB930	0929	ShouYi	Remove no use item of crystal circuit.	Delete Y5, C94, C1783.	0.2
ER31	29#	VGA DC/DC Interface	0929	ShouYi	Prevent R1792 for big current damage.	Change R1792 to 10K.	0.2
ER32	29#	VGA DC/DC Interface	0929	ShouYi	For +3VSG voltage issue on power off status.	Change R1794 to 200.	0.2
ER33	12#	PCH SATA,HDA, SPI,LPC	1004	ShouYi	For Crystal Vendor's recommendation.	Change C204,C207 from 12pF to 18pF.	0.2
ER34	32#	LAN RTL8111F	1004	ShouYi	For Crystal Vendor's recommendation.	Change C89,90 from 20pF to 12pF. Change Y2 to SJ10000E800.	0.2
ER35	13#	PCH PCIE,SMBUS,CLK	1004	ShouYi	For Crystal Vendor's recommendation.	Change C288,C243 from 20pF to 12pF. Change Y3 to SJ10000E800	0.2
ER36	20#	N13P PEG & DAC	1004	ShouYi	For Crystal Vendor's recommendation.	Change C1735,C1736 from 18pF to 12pF. Change Y4 to SJ100009700.	0.2
ER37	41#	DC/DC Interface	1004	ShouYi	Improve the +5VS charge current.	Change R428 from 220 to 10 ohm.	0.2
ER38	15#	PCH PCI,USB,NVRAM	1005	ShouYi	Change resistor type to from RP type to 0201.	Change RP1,RP2,RP3 to 0201 size. (R1900-R1910)	0.2
ER39	35#	PCIe USB3.0 ASM1042	1006	ShouYi	For crystal vendor's recommend.	Change Y9 for cost down. Change C1004, C1006 to 12pF.	0.2
ER40	37# 39#	FAN/PWRBTN/PCB PN EC ENE KB930	1006	ShouYi	For Power team's requirement.	Change the +3VLP to +3VL.	0.2
ER41	05#	CPU PM,XDP,CLK	1006	ShouYi	Reserve pull high +3V_PCH to U1.	Change the +3VS to +3V_PCH.	0.2
ER42	13#	PCH PCIE,SMBUS,CLK	1006	ShouYi	Reserve pull down to GND for Deep S3.	Reserve R1911 to GND.	0.2
ER44	41#	DC/DC Interface	1012	ShouYi	For EMI's requirement.	Add R1781, R1730 0.1uF to GND.	0.2
ER45	32#	LAN RTL8111F	1012	ShouYi	For EMI's requirement.	Change RL437,RL438 to C268,C311 (0.1uF).	0.2
ER46	06#	CPU DDR3	1020	ShouYi	For Deep S3 modified.	Change R63 to un-stuff. Change R1720 to stuff.	0.2
ER47	09#	CPU PWR/VSS	1020	ShouYi	For EMI's requirement.	Add C236.	0.2
ER48	09#	CPU PWR/VSS	1020	ShouYi	For Intel review feedback item.	Add R280	0.2

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
ER49	10#,11# 36#,37#,31#		1020	ShouYi	Change size from 0603 to 0402.	C121,C132,C134,C143,C145,C148,C158,C160 C169,C171,C1680,C1779,C1780,C500	0.2
ER50	12#		1020	ShouYi	For crystal's recommend.	Change Y1 to SJ10000DM00	0.2
ER51	15#	PCH PCI,USB,NVRAM	1020	ShouYi	For Intel review feedback item.	Add R271 to +3VS.	0.2
ER52	14#,16#		1020	ShouYi	For Deep S3 circuit modified.	Add R751,R230. Reserve R805,R804,R803,R802,R801,R800	0.2
ER53	17#	PCH PWR	1020	ShouYi	For Intel review feedback item.	Change L24 to R304.	0.2
ER54	18#	PCH PWR	1020	ShouYi	For Intel review feedback item.	Change L13 to R290.	0.2
ER55	05#	CPU PM,XDP,CLK	1020	ShouYi	For EMI's requirement.	Add R30.	0.2
ER56	22#	N13P LVDS TMDS	1020	ShouYi	For NV's recommend.	Change R1620 to 45K.	0.2
ER57	39#	EC KB930	1020	ShouYi	For Deep S3 reserve circuit.	Modified EC GPIO.	0.2
ER58	20# 39#	N13P PEG&DAC EC KB930	1020	ShouYi	For dGPU thermal throttling.	Add R430. Change R677 to unstuff.	0.2
ER59	12# 39#	PCH SATA,HDA,SPI. EC ENE KB930	1020	ShouYi	SPI flash data crisis prevention.	Add Q71, Reserve R137 and R135.	0.2
ER60	30# 32# 33# 34#	LVDS & CRT ; LAN HDMI ; HD Audio Codec	1024	ShouYi	Change IO connector symbol.	Modify JHDMI, JHP, JMIC Modify JCRT, JLAN	0.2
ER61	32#	LAN RTL8111F	1028	ShouYi	For EMI's requirement.	Change UL2 to SP050007G00	0.2
ER62	34# 36#	HDMI USB2/USB3	1028	ShouYi	For EMI's requirement.	Change D12,D13,D41,D42 to SC300002C00	0.2
ER62	30#	LVDS & CRT	1028	ShouYi	For EMI's requirement.	Change DV1,DV2,DV4,DV5 to SCA00001L00	0.2
ER63	33#	Audio Codec ALC269	1028	ShouYi	For EMI's requirement.	Change D21,D25,DA3 to SCA00001I00	0.2
ER2-01	38#	KB/TP/LED/FUNC/LID	1122	ShouYi	For change Click Pad from Glide Pad.	Add PCH_SMBDATA&CLK & GP_INT signals	0.3
ER2-02	13#	PCH PCIE,SMBUS,CLK	1122	ShouYi	For change Click Pad from Glide Pad.	Add SMBALERT# signals page connect	0.3
ER2-03	39#	EC ENE-KB9012	1122	ShouYi	For change Click Pad from Glide Pad.	Change TP_CLK&DATA pull up to +3VS.	0.3
ER2-04	34#	HDMI/Level Shift	1122	ShouYi	For HDMI LOYALTY.	Add HDMI 46@ for HDMI logo.	0.3
ER2-05	15#	HDMI/Level Shift	1125	ShouYi	For +3VSG leakage current.	Change R271 to un-stuff. Add R272 to GND.	0.3
ER2-06	12#	PCH SATA,HDA,SPI,LPC	1205	ShouYi	For Crystal vendor's requirement.	Change C204 from 18pf to 15pf.	0.3
ER2-07	35#	USB3.0 ASM1042	1205	ShouYi	Modify the USB3.0 power sequence.	Change R1040 to 51K. Change C1011 to 2.2uf.	0.3
ER2-08	38#	KB/TP/LED/FUN/LID	1205	ShouYi	Change LED/B connector and modify the schematic.	Change JFUN to 22pin and modify the circuit.	0.3
ER2-09	12#	PCH SATA,HDA,SPI,LPC	1209	ShouYi	Add SPI-ROM for WIN8	Add SA000039A20 to U59 location.	0.3
ER2-10	17# 40#	PCH PWR MINI CARD	1212	ShouYi	Change Cap for cost down.	Change C295 & C1785 to SE000000H10.	0.3
ER2-11	29# 41#	VGA DC/DC DC/DC	1212	ShouYi	Change Cap for cost down.	Change C338,C1709,C1771,C1776 to SE000000K80.	0.3
ER2-12	09# 13# 17# 18# 36#		1212	ShouYi	Change Cap for cost down.	Change C210,C211,C212,C215,C234,C235,C240,C244,C257, C262,C263,C266,C271,C277,C278,C279,C284,C324, C525,C580,C1043,C1044,C1589,CC15,CC16,CC17, CC18,CH33,CH34,CH54. SE102104K00 to SE076104K00.	0.3
ER2-13	12#	PCH SATA,HDA,SPI,LPC	1212	ShouYi	For improve S5 power consumption.	Change R199,R198,R200 to Un-stuff.	0.3
ER2-14	16#	PCH GPIO,CPU,MISC	1212	ShouYi	For HW design. (EMI's requirement change USB port)	Change R309 to un-stuff. Add R812, for PCH_GPIO22 pull down. (debug port)	0.3
ER2-15	20#	N13P PEG&DAC	1212	ShouYi	For HW design.	Change R1602 pull up to +3VSG.	0.3
ER2-16	39# 14#	EC ENE KB9012 PCH DMI,FDI,PM	1212	ShouYi	For HW design.	Change R1824 to un-stuff. Change R248 to stuff.	0.3
ER2-17	15#	PCH PCI,USB,NVRAM	1212	ShouYi	For EMI's requirement change the USB port.	Modified the USB port.	0.3
ER2-18	36#	USB2/USB3	1212	ShouYi	For HW design.	Modified the USBAI_PEN#R signals design.	0.3
ER2-19	36#	USB2/USB3	1212	ShouYi	For EMI's requirement change the USB port.	Modified the USB port.	0.3
ER2-20	34#	HDMI	1212	ShouYi	For EMI's requirement.	Reserve C641~C648 for EMI.	0.3
ER2-21	29# 41#	VGA DC/DC DC/DC	1212	ShouYi	For HW design. (single channel MOS change to dual channel)		0.3
ER2-22	30#	LVDS & CRT	1212	ShouYi	For EMI's requirement.	Modified the USB port signals.	0.3
ER2-23	32#	LAN RTL8111F	1212	ShouYi	For HW design. (single channel MOS change to dual channel)	Change the QL53 and QL52 to Q94.	0.3
ER2-24	30#	LVDS & CRT	1214	ShouYi	For EMI's requirement.	Add L9,R126,R1897.	0.3
ER2-25	22#	N13P LVDS&TMDS	1214	ShouYi	For Vendor's requirement.	Modified the X76 BOM for VGA and VRAM.	0.3
ER2-26	38#	KB/TP/FUN	1214	ShouYi	For EMI's requirement.	Add L10,R1912,R127.	0.3

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